DESIGN TECHNIQUES TO ENHANCE NOISE TOLERANCE IN CMOS DIGITAL DYNAMIC CIRCUITS

by

FERNANDO MENDOZA HERNÁNDEZ

A dissertation submitted in partial fulfillment
of the requirements for the degree of Doctor in
Sciences with specialty in Electronics in the National
Institute for Astrophysics, Optics
and Electronics

Supervised by

Dr. Mónico Linares Aranda INAOE
Dr. Víctor H. Champac Vilela INAOE

Tonantzintla, Pue.

August 21, 2003

Abstract

This thesis deals with the capacitive coupling noise problem in the dynamic digital circuits. The effects of coupling noise on delay, power consumption and signal integrity in digital submicron circuits are analyzed. A new noise tolerant dynamic digital circuit technique is proposed and its efficiency is verified and compared with previous techniques. simulation results show a noise immunity improvement in the proposed technique. This makes this new technique suitable for submicron systems. Also, the noise tolerance scaling trends are analyzed for the case of conventional and noise tolerant dynamic gates. Finally A test circuit was fabricated to validate the proposed technique. Experimental results agree quite well with theoretical ones.

Acknowledgments

I would like to thank my advisors, Dr. Mónico Linares Aranda and Dr. Víctor H. Champac Vilela for their guidance and support throughout my graduate studies, their support is gratefully acknowledged. I would also like to thank Dr. José Alejandro Díaz Méndez, Dr. Miguel Angel García Andrade, Dr. Roberto S. Murphy Arteaga, Dr. Kaushik Roy and Dr. Alfonso Torres Jácome for their feedback on the dissertation and for serving on my committee. I thank all professors that gave me an advice and taught me the art of IC design. Thanks also to the Instituto Nacional de Astrofísica Óptica y Electrónica for giving me the opportunity and support to do my research. Thanks also to the efficient administrative staff who always helped me with a smile. I also wish to thank all friends that helped me in my graduate studies, thanks Antonio Zenteno for the support on Cadence.

Also many thanks to the Consejo Nacional de Ciencia y Tecnología for the grant that helped me to conclude my graduate studies. This work was supported in part by the Consejo Nacional de Ciencia y Tecnología (CONACyT) under grant No. 34557-A.

Dedicates

To my lovely wife Luz Ilía and my dear son Alan Fernando.

For their love, support and encouragement. Both of you have made the last two years wonderful and I look forward to many more together. You are the main reason of my effort.

To my parents Justina and Fernando.

For their ever love and support which helped me to reach my objectives. Both of you have always being close to me and your support is gratefully acknowledged.

To my sister and brothers Cielo, Iván and Jesús.

For their love, friendship and support. Many thanks sister and brothers for a lifetime of friendship and fun, we make a beautiful team.

Contents

Preface

The increased use of portable and wireless systems with very low power budgets and the need for microprocessors with high operation speed is the cause of the impressive advancement of the VLSI circuit technology. The driving force behind this advancement is the rapid scaling of the dimensions of the transistor. Due to this scaling more complex systems with high-speed operation can be integrated in a single chip. To reduce power consumption, especially in portable and wireless systems with very low power budgets, the supply voltage is scaled. Threshold voltage also needs to be scaled to preserve the performance of the circuits. However, when the threshold voltage is scaled subthreshold leakage currents are increased [1]. As technologies scale, more systems can be packaged on a chip. To integrate an increasing number of devices in a chip interconnections are being scaled down in cross section to place more interconnections closed together whereas wiring levels have been growing. By increasing the height and width in global interconnections RC delay can be reduced, this is sometimes referred to as reverse scaling. However, some wires are not being scaled in length. This causes drawbacks especially on global delay and signal integrity.

For future technologies the maximum interconnect length, with a fixed geometry, that can be switched in a clock period is a decreasing fraction of the chip-side length. The fraction of cycle time wasted by the interconnections is increased with every technology generation. The energy dissipated by these interconnections is also increased. These drawbacks are a challenge in future technologies.

Signal integrity issues are a main concern in high performance circuits. Large interconnections placed close together, higher clock frequencies, and the increased aspect ratio of the wires increase the capacitive coupling between them. This coupling can generate spurious noise pulses

on a, otherwise, stable interconnection if other coupled interconnections have a signal transition. These noise pulses can propagate and arrive at the inputs of logic gates. Consequently, logic failures can occur and the reliability of the systems is degraded.

The need for high performance systems with increased noise tolerance is evident. It is necessary to design noise tolerant circuit techniques that bear noise effects with slight performance penalties. These noise tolerant techniques are useful especially in those parts of the systems where there is an increasing rate of data like in datapaths.

Chapter 1
INTRODUCTION

The rapid advancement of the VLSI circuit technology is due to the increased use of portable and wireless systems with very low power budgets and to the need for microprocessors with high operation speed. To achieve this advancement the dimensions of the transistor are rapidly scaling. Due to this scaling more complex systems with high-speed operation can be integrated in a single chip. To reduce power consumption, especially in portable and wireless systems with very low power budgets, voltage supply is scaled. Threshold voltage also needs to be scaled to preserve the performance of the circuits. However, when the threshold voltage is reduced leakage currents are increased. To integrate an increasing number of devices in a chip it is necessary to have more interconnections close together. However, large interconnections placed close together, higher clock frequencies, and the increased aspect ratio of the wires increase the capacitive coupling between them. This coupling can generate spurious noise pulses on a, otherwise, stable interconnection if other coupled interconnections have a signal transition. These noise pulses can propagate and arrive at the inputs of a logic gate. Consequently, signal delay or logic failures can occur and the reliability of the systems is degraded. The increased use of dynamic logic families aggravate this problem. Signal integrity issues are a main concern in high performance circuits.

The 2002 update of *The International Technology Roadmap for Semiconductors* (ITRS) [2] refers to two Grand Challenges for the Semiconductor Industry in the near- (through 2007) and long-term (2008 and beyond). These Grand Challenges were classified into the two following

categories: Enhancing Performance and Cost-effective Manufacturing. In order to enhance the performance of MOS structures in the near term the leakage current must be lowered. In the long-term, among other factors, a better noise management will lead to a cost-effective manufacturing.

The 2002 update of the SIA Roadmap also points-out that the decreasing noise tolerance per technology node is becoming an important issue in the design of functional devices and systems. This fact is becoming more severe due to lower noise margins mainly in low power systems.

For future technologies the maximum interconnect length, with a fixed geometry, that can be switched in a clock period is a decreasing fraction of the chip-side length. The fraction of cycle time wasted by the interconnections is increased with every technology generation. The energy dissipated by these interconnections is also increased. All these factors make interconnection to play a significant role in VLSI design.

There are two ways to address interconnect noise issues: 1) by reducing the peak noise pulse generated in the interconnections by means of interconnect optimization (repeater insertion, wire sizing, driver sizing, etc.), and 2) by designing noise-tolerant circuits that bear the every time bigger noise pulses appearing at their inputs. So, the need for high performance systems with increased noise tolerance is evident. It is necessary to design noise tolerant techniques that bear noise sources with slight performance penalties.

1.1 Digital Noise Sources

In this section some of the digital noise sources are reviewed. Noise used to be a concern of interest only in analog circuit design. In digital circuits noise was not a parameter of interest because although digital circuits create much more noise than analog circuits, they were inherently immune to noise [3]. This inherent noise immunity is due to the static high-gain restoring logic gates such as the CMOS inverter, which has a very nonlinear voltage transfer characteristic. The continued scaling of CMOS technology and the increased use of dynamic circuits, which change noise immunity by performance, have brought noise to the forefront. Noise is now an important issue even in purely digital designs.

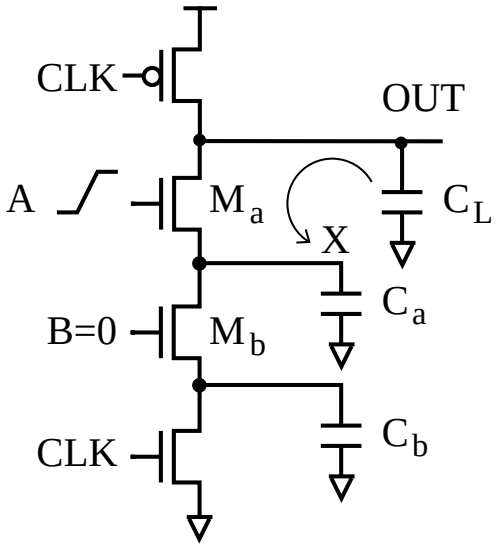


Figure 1.1: Charge sharing in dynamic circuits.

1.1.1 Charge Sharing

Charge sharing noise is a concern in dynamic gates due to the charge storage process that govern their operation. Charge sharing noise is produced by charge redistribution between the dynamic node and internal nodes of a dynamic gate. This charge redistribution occurs in the worst case when, in evaluation phase, all inputs go high except the lower one considering dynamic AND gates [4]. Consider the circuit of Fig. 1.1. During the precharge phase, the output node is precharged to voltage supply (V_{DD}), i. e., the capacitance C_L is charged. Assume that all inputs are set to LOW and that the capacitance C_a is discharged by a previous evaluation. Assume further that input B remains LOW during evaluation phase, while input A makes a LOW to HIGH transition, turning transistor M_a on. The initial charge stored on capacitor C_L is redistributed over C_L and C_a. This causes a drop in the output voltage, which can not be recovered due to the dynamic nature of the circuit [5].

With the following initial conditions: $V_{out}(t=0)=V_{DD}$ and $V_X(t=0)=0$, which are valid under the above assumptions the output voltage drop is calculated. Two cases are considered [5]:

1. $\Delta V_{out} < V_{tn}$. Where V_{tn} is the threshold voltage of NMOS transistors and the final value of V_X, the voltage at node X, equals $V_{DD} - V_{tn}(V_X)$. Under charge conservation the

following result is obtained:

$$C_L V_{DD} = C_L V_{out}(t) + C_a[V_{DD} - V_{tn}(V_X)]$$

or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L}[V_{DD} - V_{tn}(V_X)] \tag{1.1}$$

2. $\Delta V_{out} > V_{tn}$. V_{out} and V_X reach the same value:

$$\Delta V_{out} = -V_{DD}\frac{C_a}{C_a + C_L} \tag{1.2}$$

To reduce charge sharing problems C_a must be smaller than C_L. This is normally so in digital circuits.

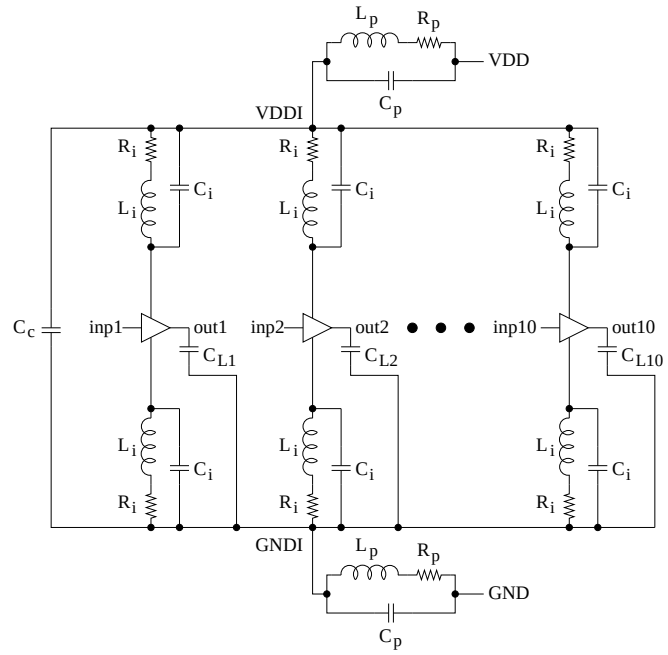
1.1.2 Ground Bounce

Due to technology trends more transistors are being integrated in an ever increasing size die, with higher speeds being achieved. These trends bring an increasing number of CMOS internal logic switching simultaneously. Also, the number of the I/O buffers switching simultaneously has increased. When CMOS logic gates switch, they draw current from the power supply bus or inject current into the ground bus. This current generates voltage variation across the unavoidable parasitic inductances that connect the IC die to the external pins. These voltage variations are referred as ground bounce or simultaneous switching noise or ΔI noise.

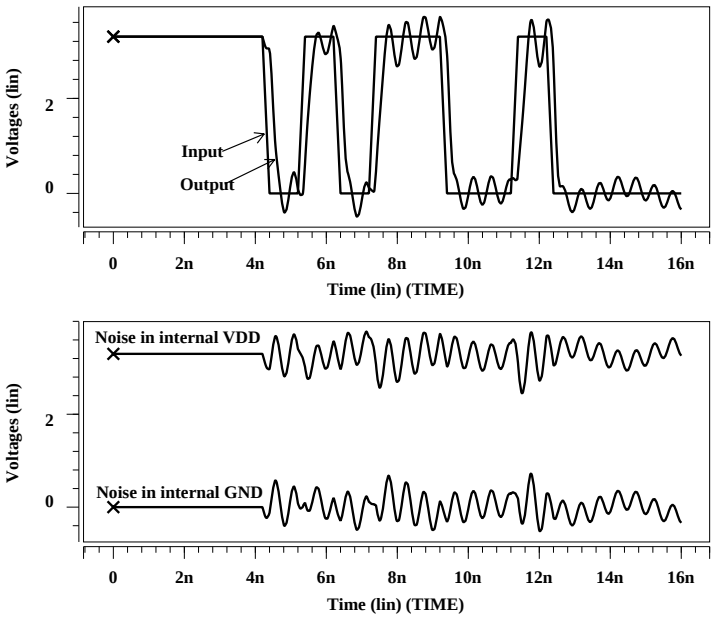
The amount of the maximum voltage drop on the power supply or ground busses can be approximated by

$$\Delta V = nL\Delta I/\Delta t \tag{1.3}$$

where n is the number of internal circuits switching simultaneously, L is the effective wire inductance of power or ground busses, ΔI is the current variation during transition, and Δt is the rise or fall time of the signals switching in the internal circuits or I/O drivers. It can be observed that if clock frequency increases, and so the transition times become shorter, or if the number of gates (n) that switch at the same time is also increasing, the maximum voltage drop (ΔV) increases. The equation 1.3 gives a first order expression for ground bounce. More accurate models have been proposed to analytically estimate the ground bounce noise [6] [7] [8].



(a)



(b)

Figure 1.2: (a) Test circuit for simulating ground bounce in internal logic, and (b) simulated waveforms for both, high to low and low to high transitions at the output of the test buffers.

Ground bounce may decrease the transistor drive capability, may reduce the noise margins or can cause logic delay failures, [9] [10]. In this way, to guarantee signal integrity it is necessary to minimize ground bounce in supply and ground lines. To reduce ground bounce in high-performance circuits several techniques and methodologies have been recently proposed [9] [10] [11] [12] [13] [14] [15] [16].

Fig. 1.2(a) shows an equivalent circuit of pins and on-chip power supply lines [10]. L_p, R_p and C_p denote the bonding and pin parasitics associated with the package. VDDI is the internal V_{DD} node that distributes power to internal circuits. C_c is the on-chip decoupling capacitance. L_i, R_i and C_i are the parasitics associated with the power bus interconnects. 10 buffers are used to simulate the voltage variations at the VDDI and GNDI nodes, each buffer has an output load capacitor C_L. The simulation results using HSPICE are shown in Fig. 1.2(b). Voltage variations are generated in the supply rails when the 10 buffers switch simultaneously and the output of buffers have resonance.

1.1.3 Leakage Current

The transistors in integrated circuits are continuously scaled down to achieve high performance. voltage supply is also scaled to assure low power consumption. When voltage supply is reduced the threshold voltage (V_t) of transistors has to be scaled down in order to maintain performance improvement [17]. However, whether the threshold voltage is decreased the subthreshold leakage current in transistors present a logarithmic increase. This increase is due to the weak inversion state leakage and is a function of the threshold voltage [18]. Subthreshold leakage current is not the only leakage mechanism in transistors, there are other leakage current mechanisms that arise as transistors are scaled down.

In total, leakage current in deep submicron transistors has six components as depicted in Fig. 1.3 [18]: 1) the reverse bias drain and source to well junctions leakage (I_1), 2) the subthreshold leakage current between source and drain for gate voltages below V_t (I_2), 3) the gate oxide tunneling current due to the reduction of gate oxide thickness (I_3), 4) gate current due to hot-carrier injection from substrate to gate oxide (I_4), 5) gate-induced drain leakage due to high electric field effect in the drain junction of MOS transistor (I_5), and 6) the channel punchthrough current (I_6).

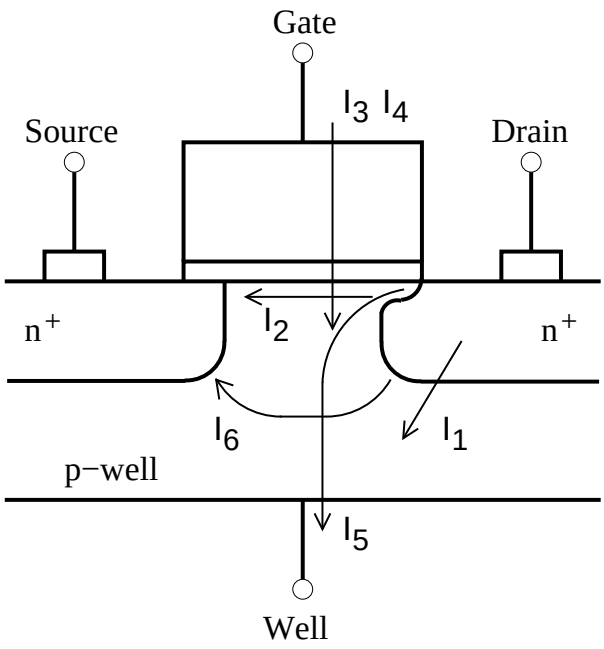


Figure 1.3: Leakage current mechanisms of deep-submicrometer transistors [18].

Leakage current contributes to the power consumption of a CMOS circuit not only in standby mode of operation but in active mode. The part of the total power dissipation determined by the leakage current is the static (leakage) power given by [18]

$$P_{LEAK} = I_{LEAK} \cdot V_{DD} \tag{1.4}$$

where I_{LEAK} is the leakage current generated by the six components listed above and V_{DD} is the voltage supply.

Techniques to reduce the leakage current can be divided into process and circuit techniques. two main process techniques are retrograde channel doping and nonuniform channel doping [18]. Transistor stacking is a circuit technique for leakage reduction.

Furthermore, leakage current can destroy the logic level in a dynamic precharge node and consequently a logic error can occur.

1.1.4 Capacitive Coupling

In order to reduce the wire resistance and therefore, the wire delay, the interconnect aspect ratio (thickness/width) is increased. However, the capacitance to neighboring wires also increases and

can be larger than the capacitance to wires above and below. In higher levels of interconnections the coupling capacitance between wires is more pronounced due to the increased wire thickness and the reduction of the substrate capacitance [19]. This coupling capacitance can exceed 70% of the total capacitance [20]. Hence, the ratio of coupling capacitance between lines in the same level to the total capacitance tends to increase as is pointed out in [21] [22]. Accordingly, capacitive noise between lines is becoming an important issue in deep submicron technologies.

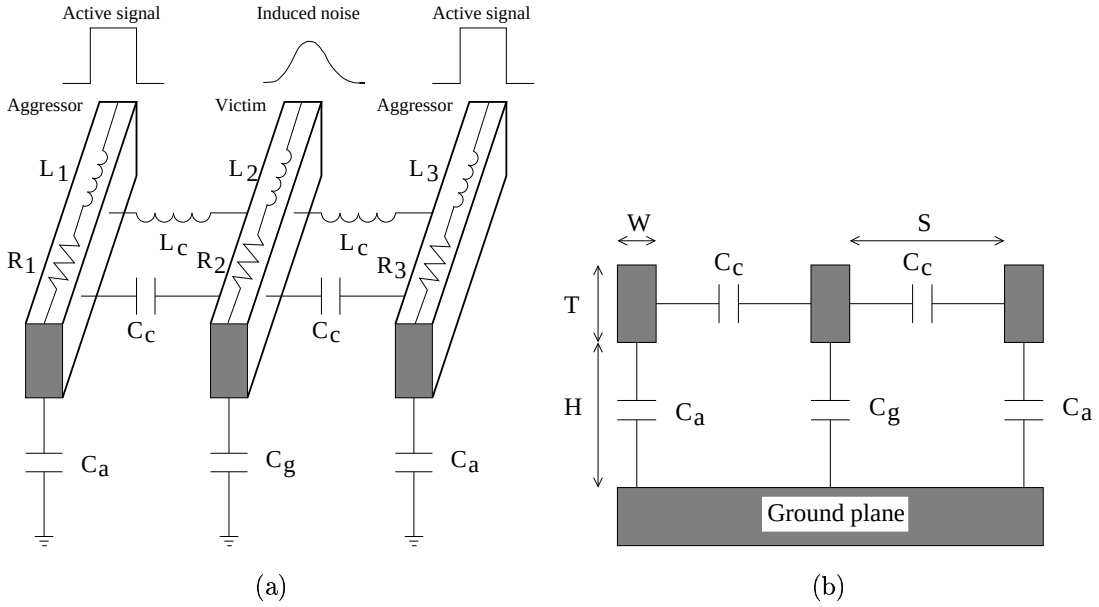


Figure 1.4: Representation of the 3-line conductor system to show the coupling noise behavior: (a) 3-D representation, and (b) 2-D representation showing the associated capacitances.

Consider the 3-line conductor system shown in Fig. 1.4. When two (aggressor) lines switch simultaneously, (worst-case), current flows through the coupling capacitors (C_c) to the quiet (victim) wire inducing noise on it. This noise comes in the form of voltage pulses that deviate the logic level of quiet nodes from its nominal V_{DD} or ground level. If the peak noise voltage at the victim wire is greater than the threshold voltage, a logic failure can occur. Furthermore, extra power consumption and larger delay are caused by the momentary glitches within the logic gates.

A first-order model for this coupling noise, also known as crosstalk, is [20]

$$V_n = V_{dd}\left(\frac{C_c}{C_c + C_g}\right)\left(\frac{1}{1+\frac{\tau_{att}}{\tau_{vic}}}\right) \tag{1.5}$$

where τ_{att} and τ_{vic} are, respectively, the time constants of the aggressor and victim drivers. If the aggressor has a much smaller time constant than the victim (and is hence much stronger), the noise approaches a pessimistic worst case. However the transition times of different gates are balanced and the time constant ratio is greater than one [20]. It is obvious that interconnection scaling trends trade off signal integrity by circuit performance. To balance this trade off the use of repeaters in the interconnections is useful. As stated by Sylvester [23] at 0.18μm and beyond both local and global interconnections can have less delay penalty using repeaters. Even more, the use of repeaters reduce the crosstalk noise in the interconnections because a larger driver has a lower resistance and a much smaller time constant. Thus, less crosstalk is generated for the same coupling capacitance at the expense of increasing power and area consumption.

1.2 Interconnect Scaling Trends

To satisfy the requirements of consumer electronics the VLSI circuit technology has advanced in an impressive manner. This advancement has been possible due to the rapid scaling of the feature size, i.e., the minimum dimension of the transistor.

The first scaling scheme was the constant field scaling [24]. As the transistor and interconnects are scaled down in size by a factor S the same electric-field patterns are achieved. This is because the voltage supply is scaled and the impurity doping concentration is increased by the same factor S.

With constant field scaling the transistor density improves by a factor S^2 due to the smaller wiring and device dimensions. Next, the transistor switching time is reduced which implies higher operation frequency. Finally, the power dissipation in each module is reduced because the voltage and current in each transistor are reduced by a factor S. Considering that the scaling enables much higher degree of on-chip integration, the power density remains constant.

Two kinds of wires are distinguished regarding wire delay under technology scaling [20]: local and global wires. Local wires are used to connect logic gates within blocks, and when

transistors and blocks shrink, these wires scale. Global wires connect many blocks and usually span a significant part of a die. Due to increase in the density and size of the die, these wires actually become larger (reverse scaling).

In the scaling process, resistance in the local wires grows since the width and height both scale down and capacitance decreases very slowly due to the use of low-k dielectrics. Consequently, the delay time of local wires remains the same. Resistance and capacitance in the global wires also increase due to the growth in die size, hence, the delay of global wires increases at a faster pace, which results in important interconnect performance degradation [20] [25] [26].

It is evident that the scaling of wires, unlike transistors, does not enhance their performance. Interconnect delay is becoming a significant fraction of the cycle time [27] and even with constant dimension global wires the maximum wire length that can be switched in a clock cycle is a decreasing fraction of the die side length [22].

Reverse scaling of global interconnections alleviates the wire problem. In this scaling scheme interconnection dimensions are increased in the same rate as the chip size. As a result, the resistance decreases and the capacitance grows, resulting in a constant RC delay at the expense of wire density [25]. New interconnect materials such as copper (Cu) and low-k dielectrics are used to alleviate the interconnect performance degradation. Cu, with its lower resistivity than aluminum (Al) and with its excellent electromigration resistance and relatively low cost, becomes a better choice than aluminum. Low-k dielectric materials reduce the parasitic capacitances between interconnections. Consequently, the combination of a low-k insulator and Cu will lead to performance improvement and cost reduction. However, some authors have argued that this solution alone may not be sufficient nor cost effective to solve the wire problem [22] [23].

A new metallization scheme known as Dual Damascene meet these performance needs [28]. Dual Damascene is a wiring technology for forming interconnect patterns based on copper metal lines inlaid into dielectric layers, then polishing away the excess metal on the wafer surface [29]. Cu interconnections are very difficult to pattern by conventional approach. Dual Damascene patterns Cu interconnections more easily by applying modified process steps. New low-k dielectric materials can be easily used as inter-layer and intra-layer insulator. Dual Damascene technology offers an enhanced manufacturing yield due to its planarity. The interconnect reliability is improved by reducing electromigration concerns. The reduced RC losses and reduced

contact resistance benefit the performance of Dual Damascene interconnections [28].

Copper/low k interconnects formed by the dual damascene technique can be used in manufacturing either DRAM or logic devices.

1.3 Scope of the Thesis

This thesis deals with capacitive coupling noise (*crosstalk*) effects in deep-submicron dynamic digital circuits. Crosstalk effects in dynamic circuits are analyzed. A new noise tolerant dynamic digital circuit technique is established and its performance is analyzed in terms of delay and power consumption. The noise tolerance of this proposed technique is studied and compared with previous noise tolerance techniques. To achieve these objectives, the thesis is organized as follows.

Chapter 2 presents a review of logic families with emphasis in dynamic logics (Domino, TSPC, ANL). Their operation is described as well as advantages and drawbacks. These techniques present high performance at a cost, they suffer low noise tolerance. Thus, it is necessary to understand the operation of these dynamic logics to propose methods to alleviate their noise problems.

Chapter 3 examines the basic concepts of digital noise. The metrics for power consumption, delay, and noise tolerance are revised and explained. Crosstalk noise effects on dynamic circuits are analyzed and existing noise tolerance dynamic circuit techniques are reviewed.

Chapter 4 introduces a new noise tolerant dynamic circuit technique. Its structure and operation are described and the noise tolerance mechanism of the proposed technique is analyzed. To verify the effectiveness of the proposed technique it is applied to AND- and OR-type dynamic logic gates and it is compared with recently proposed noise tolerant techniques. This comparison takes into account the noise tolerance improvement as the main design parameter. Power consumption and delay are drawbacks that should be minimized in order to make the technique efficient and useful. A 4-bit carry look-ahead full adder is designed with the proposed technique and its noise tolerance and performance are compared with a conventional dynamic full adder. This example confirms the effectiveness of the proposed technique. The proposed technique is applied to TSPC and Domino dynamic logics to demonstrate its flexibility. Also,

a study of the noise tolerance scaling trends of the proposed technique along with conventional dynamic logic and other noise tolerant technique is presented to analyze the effectiveness of the proposed technique with technology scaling. Finally, an improvement of the proposed technique is introduced and, by means of an example, a first analysis of its noise tolerance and performance is given.

Chapter 5 gives experimental results of the proposed technique performance and noise tolerance. A test circuit is designed and fabricated to test the increased noise tolerance in pipelined circuits. The CAD design flow used is described and the normal operation and operation under noise of the test circuit are analyzed.

Chapter 6 summarizes the results of this research and suggests future work topics.

Chapter 2
OVERVIEW OF LOGIC FAMILIES

Speed and power consumption are two important design constraints in current integrated circuits. Speed has become an important requirement in high end microprocessors. Power consumption is crucial in the design of portable applications such as mobile phones. Area used to be a design constraint. Currently, area is not a main design constraint due to the high integration levels. Furthermore, noise has emerged as an important issue in deep submicron technologies. In this way, the design requirements determine the use of either static or dynamic logic families.

2.1 Static Logic Families

In a static logic circuit the output is always driven to ground or voltage supply levels. Also, the output is only function of the input, i.e., the circuit is not synchronized by a clock signal. Static logic has low sensitivity to noise. It may recover from noise induced logic errors whether there is no loop in the circuit. Static logic also has an acceptable power consumption and good speed. The drawbacks are that complex static CMOS gates consume more area and are slow for certain applications.

2.1.1 Static Complementary MOS

Static complementary MOS is the most common static logic family and is divided into a pull-down network composed of NMOS transistors and a pull-up network made of PMOS transistors

[30]. Both networks, shown in Fig. 2.1, are complementary so that the output has always a direct path to power supply or ground. A clear drawback of static CMOS is the increased input load because each input must drive both NMOS and PMOS transistors. Furthermore, PMOS transistors are slower than NMOS transistors since the mobility of holes is smaller than that of electrons. Therefore, PMOS transistors need to be sized bigger than NMOS ones.

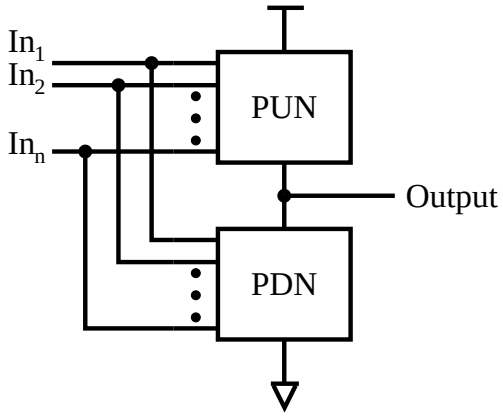


Figure 2.1: A general static complementary CMOS gate.

2.2 Dynamic Logic Families

In VLSI design faster circuits are required to manage the always growing amount of data. Dynamic circuits are commonly used in both data path and random control structures [31]. Dynamic circuits use charge storage as a means of holding output state, which is function not only of the input but of the clock signals. A general scheme of a basic dynamic CMOS gate is shown in Fig. 2.2. The operation of this circuit is divided into two phases: *precharge* and *evaluation*. The phases are controlled by the clock signal CLK. In the precharge phase the clock goes low and the output, known as the dynamic precharge node or simply dynamic node, is precharged to voltage supply by the PMOS transistor M_P or remains high. If during that time the pull down network turns ON, no direct path to ground exist because the NMOS transistor M_e is OFF (see Fig. 2.2). Thus the precharge transistor and the pull down network (PDN) do not operate at the same time and no dc power is consumed. During the evaluation phase the clock goes high, the PMOS transistor M_P is turned OFF and the NMOS transistor M_e is turned ON. The output discharges or remains in the previous state depending upon the PDN

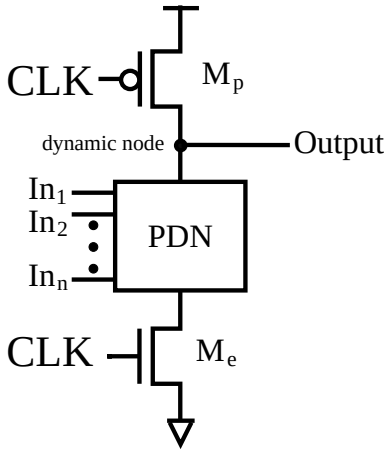


Figure 2.2: A general dynamic CMOS gate.

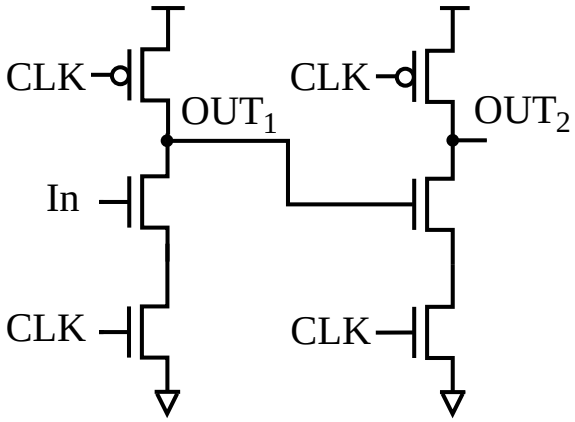


Figure 2.3: Cascading dynamic CMOS gates.

structure and the values of the inputs.

One drawback arises when dynamic logic is tried to cascade because dynamic gates cannot drive other dynamic gates. Fig. 2.3 shows two dynamic gates in series. In precharge phase (CLK=0) both dynamic gate outputs are precharged high and the PDN of the second dynamic gate is turned ON. Suppose that the input of the first dynamic gate makes a low to high transition. At the beginning of the evaluation phase (CLK=1) the output of the first dynamic gate discharges. While this output is discharging the output of the second dynamic gate is also discharging because the PDN is ON. This process continues until the output of the first dynamic gate equals V_t and the PDN of the second dynamic gate is turned OFF. At this point the output

of the second dynamic logic is at an intermediate voltage level causing a false logic level. The problem came from the fact that the output of the first dynamic gate is precharged to 1 and during evaluation phase can only make high to low transitions while a low to high transition is required at the inputs.

Adding a static inverter at the output of the dynamic CMOS gate is the common strategy to solve the problem of cascading dynamic logic gates, this is the case for the domino logic family [32]. By doing this the output of the static inverter is low in precharge phase because the dynamic gate has been precharged to high. With this addition correct operation is guaranteed because the inputs to the next gate will make a low to high transition during the evaluation phase.

2.2.1 Standard Domino Logic

A domino gate [32] consists of two parts. The first part is the dynamic CMOS gate previously discussed and the second one is a static CMOS inverter, as shown in Fig. 2.4 for a general case. Only the output of the dynamic CMOS gate is connected to the inverter and the inverter output is connected to the fan-out of the gate. This is advantageous because the fan-out of the gate is driven by a static inverter with a low impedance output, so noise immunity is increased. Furthermore, the inverter can be sized to drive a large fan-out and thus optimize the speed. Domino logic has no static power dissipation and little area is needed to implement systems using Domino logic. Finally, the output of the dynamic gate is isolated from the fan-out. Hence, the dynamic node capacitance is isolated from the load capacitance.

The operation of a chain of domino gates is as follows (see Fig. 2.5). In precharge phase (CLK=0) the dynamic node of every gate is set high, thus the inverter output is set low. This means that all inputs of the internal gates are low at the beginning of the evaluation phase satisfying the requirement that the inputs can only make a low to high transition during the evaluation period [5]. During evaluation phase (CLK=1) the outputs of the first column of domino gates make a low to high transition or remain low, depending on the inputs state. If all inputs in the first column of domino gates go high then the corresponding outputs go high and the second gate turns ON, affecting the third gate. This process continues until the whole chain is evaluated like in a line of falling dominos, hence the name.

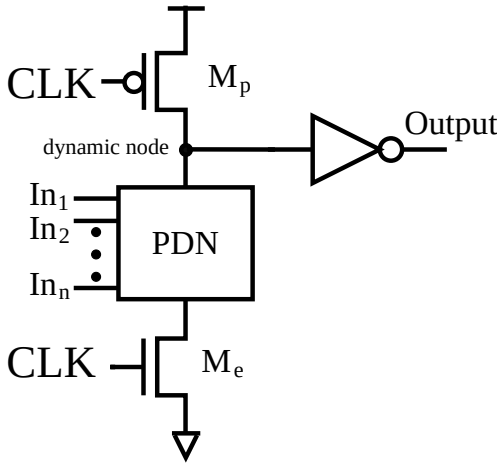


Figure 2.4: A general domino CMOS gate.

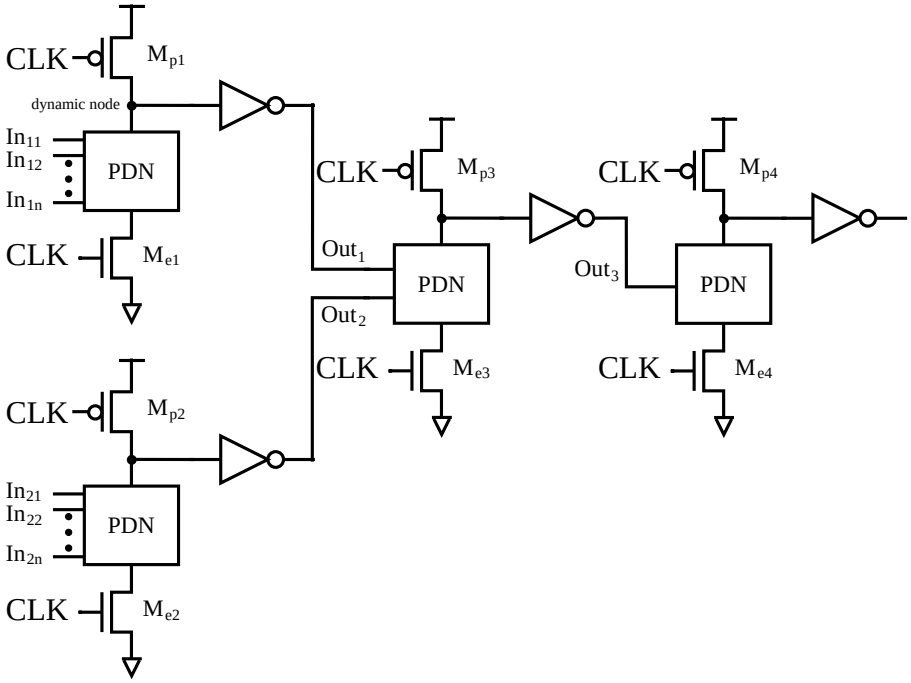


Figure 2.5: Domino CMOS logic.

In domino circuits all gates can be synchronized with the same clock edge. High speeds can be achieved because the high to low transition is zero (as the output node is precharged zero) and the load capacitance is small (only one gate capacitance per input).

Limitations of this logic family are evident: First, only noninverting gates can be used. This represents a problem when complementary inputs need to be used, like in the case of an XOR gate. Second, some input combinations can arise charge sharing problems and the level of the dynamic node could erroneously go low, setting high the inverter output.

Domino logic has been used in the design of high speed microprocessors like the SPARC V9 [33] and the Itanium 2 [34].

2.2.2 True Single Phase Clocking (TSPC) Logic

Many work have been done to solve the problems associated with the conventional dynamic CMOS latches, namely data races due to clock skew, area overhead and two or more phase clock signals [35] [36]. Although these logic families solve the first two problems, they operate with a two phase clock. Because this, large area and significant power consumption is expended in the clock distribution network. True single phase clocked logic (TSPC) [37] [38] is the first result in the search process for counteracting these drawbacks.

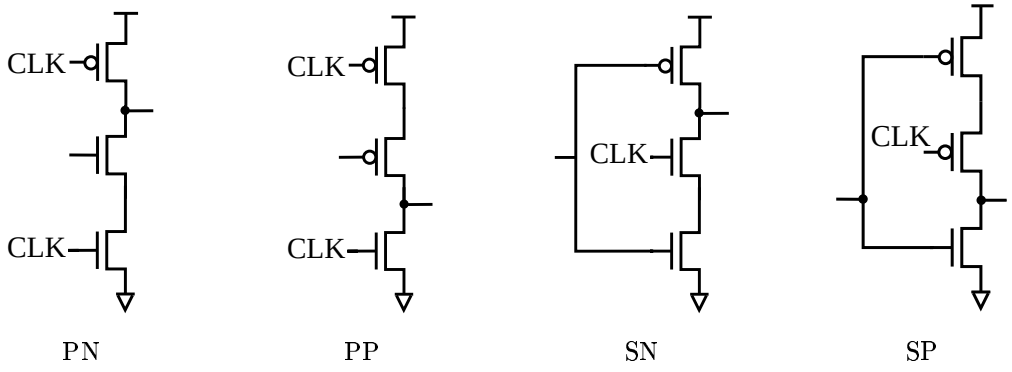


Figure 2.6: Four basic stages in TSPC.

There are four basic stages in TSPC logic: precharge n- and p-stages and non-precharge n- and p-stages, named PN, PP, SN and SP stages, respectively (see Fig. 2.6). An N-block (or N-latch) can be formed, in its precharge version, by a combination of PN+SN, Fig. 2.7(a). In

the same way a precharge P-block can be formed by a combination of PP+SP, Fig. 2.7(b).

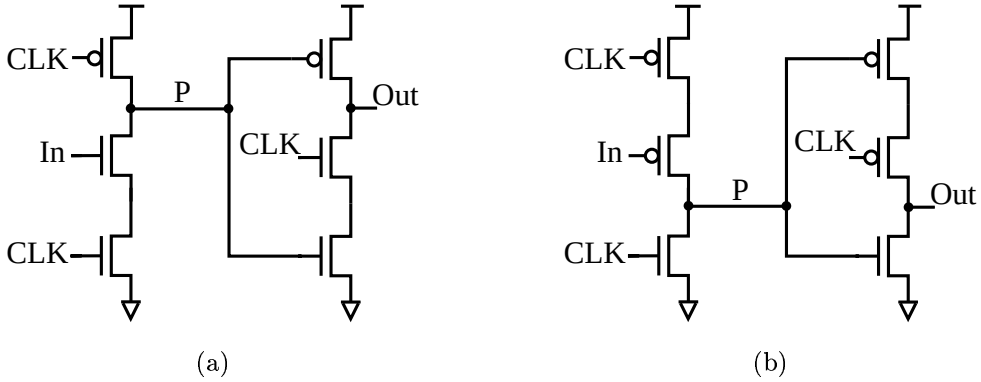


Figure 2.7: TSPC precharge latches: N-latch (a), and P-latch (b).

A non-precharge version of N-block can be formed by a combination of SN+SN, as shown in Fig. 2.8(a). P-block is formed, in its non-precharge version, by a combination of SP+SP, see Fig. 2.8(b).

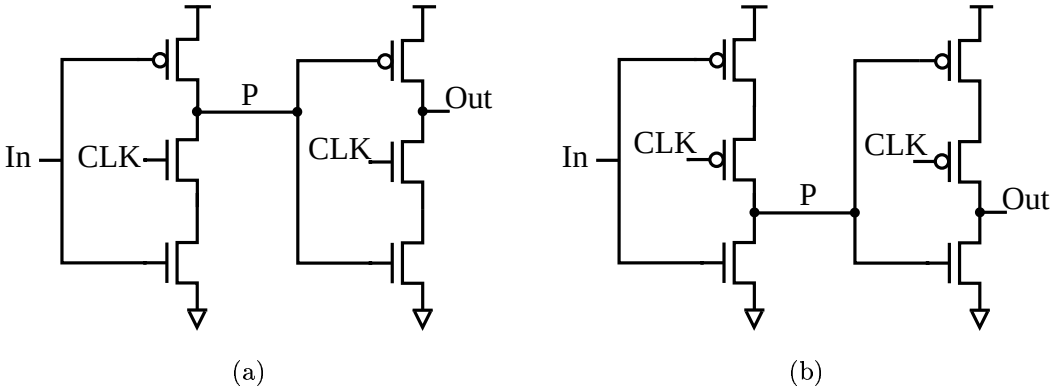


Figure 2.8: TSPC non-precharge latch: N-latch (a), and P-latch (b).

The operation of the precharge N-latch, Fig. 2.7(a), is explained as follows. When the clock is low (precharge phase) the dynamic node P is precharged high and the output is in a high impedance state and therefore it is stable (races are thus eliminated). At the clock transition low to high the pull-down network (PDN) of the N-block is evaluated: if it is ON, the node P starts to discharge and the output becomes high, latching the inputs. If it is OFF, the node

P remains high and the output goes low or remains in its previous state. When the clock is low again, the node P is precharged high and the output retains the previous logic level. The operation of the P-latch is similar to that described here.

The operation of the non-precharge N-latch, 2.8(a), is described as follows. When CLK is low (precharge phase) the pull-down networks of the two N-C^{2}MOS stages are disabled and, depending on the input data, the pull-up network of the first N-C^{2}MOS stage can be activated. Whether the input is high the precharge node P will be in a high impedance state preserving the previous logic level, whether the input is low the precharge node P will be high and the output will be in a high impedance state. In both cases the output is isolated from the input and races are thus eliminated. When CLK is high (evaluation phase) the N-latch acts as two cascaded inverters being transparent and noninverting, thus the output will take the level of the input. The operation of the P-latch is similar to that described here.

An N-latch can't drive another N-latch using the same clock. However, a P-latch solves this problem because works exactly as an N-latch using the inverted clock. In this manner a pipeline can be formed by alternately placing a P-latch and an N-latch. Logic function blocks can be included in the P- and N-latches or placed between them, as shown in Fig. 2.9, depending on the logic type and inversion requirements.

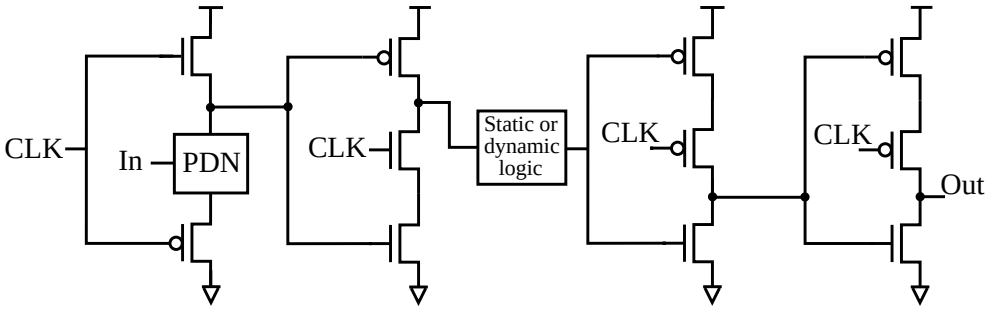


Figure 2.9: TSPC precharge latches with included logic.

The switching factor of the clock signal is α_{CLK}=1 and the switching factor of the node P in precharge logic may be as high as α_P=0.5 [39]. Furthermore, precharge latches have one additional clocked transistor than non-precharge ones. These facts contribute to the higher power consumption of the precharge latches than the non-precharge ones. On the other side, precharge latches use less transistors than the non-precharge does and the inputs have less

capacitive load. Because this, they are adequate for high speed applications. Other advantage of precharge latches is that charge redistribution problems are less likely to occur. Contrarily, charge redistribution can affect the non-precharge latches.

The TSPC logic has the advantage that there is no even inversion constraint either between two latches or between the latch and the dynamic logic block. Another advantage is that only one clock phase is required, consequently a higher clock frequency can be reached.

Modified versions of the TSPC precharge latches shown in Fig. 2.7 are depicted in Fig. 2.10 [38]. These modified precharge latches avoid the glitches at the output, which are a characteristic of precharged TSPC logic. However, the modified precharge P-latch, Fig. 2.10(b) can be slower than the original precharge P-latch because the PUN of its output stage has three transistors instead of two [see Fig. 2.10(b)].

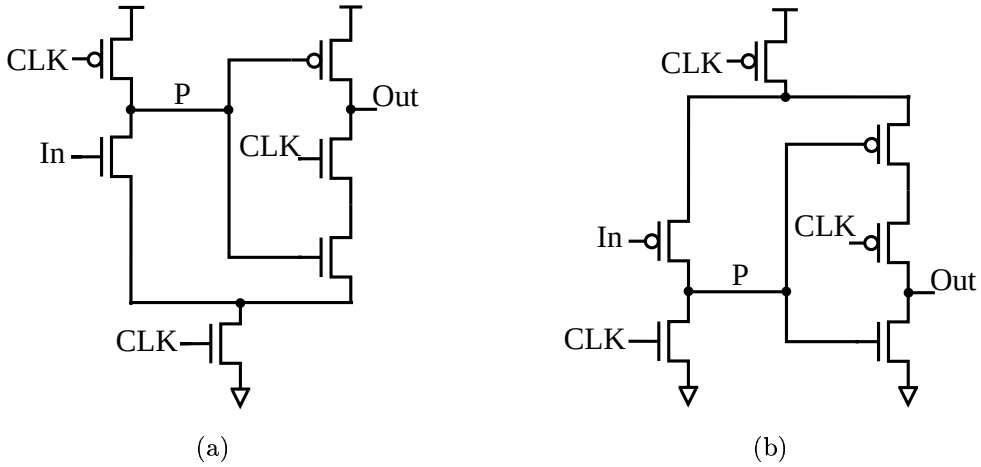


Figure 2.10: Modified precharge latch stages: N-latch (a), and P-latch (b).

The non-precharge logic blocks can be simplified into the circuits of Fig. 2.11 called split-output latches [38] where only one transistor is controlled by the clock. This implies that the clock load is reduced by half with respect to the non-precharge version. The problem with the split-output technique is the poor drive capability of the output stage because the same transistor is required to transmit both high and low levels.

In general, TSPC logic has no complementary signals and consequently inverted signals in an N-block come from a previous P-block. This can be a speed limitation. Modifications to

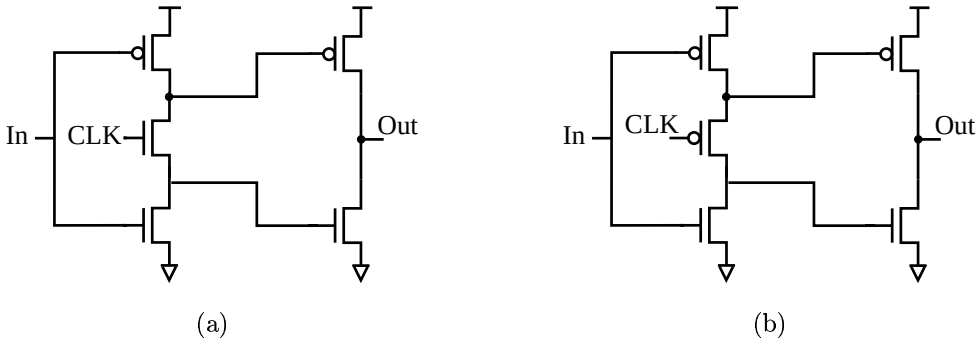


Figure 2.11: Split-output TSPC latches: N-latch (a), and P-latch (b).

the conventional TSPC logic are done in order to mitigate these bottlenecks [40]. TSPC logic, like other dynamic logics, suffers a low noise immunity [41] due to charge storage operation principle. TSPC logic has been successfully used in microprocessors [31] [42], barrel shifters [43], adders [44], prescalers [45] and accumulators [46].

2.2.3 All-N-Logic

In a pipeline system, NORA and TSPC logics use the low-speed P-block. Therefore the clock frequency is determined by the operation of the P-block. All-N-logic overcomes the disadvantage of using P-blocks that NORA logic [36] and TSPC [37] [38] have.

The basic blocks of all-N-logic (ANL1) [47] are shown in Fig. 2.12. The N1-block is a revised version of the TSPC N-latch of Fig. 2.10(a). The operation of the N1-block is as follows: when the clock is low (precharge phase) the dynamic node P is precharged through the PMOS M_{P1}, the PMOS M_{P2} is shut OFF, hence the output is in high impedance and holds the previous state. When the clock goes from low to high (evaluation phase) both NMOS M_{N1} and M_{N2} are ON. If the PDN evaluates ON, the dynamic node P is discharged to ground and the output (OUT) is high. If the PDN is OFF node P remains high and a direct path is formed from the output to ground. The precharge transistor M_{P3} overcomes the charge redistribution at the output. When both clock and the PDN are high the node P is low and the output is high, the PMOS M_{P3} turns ON and causes node "b" to charge to V_{DD}. Hence there is no charge redistribution from the output to node "b" because they are at the same voltage level.

The N2-block of the Fig. 2.12(b) is the complementary circuit of the N1-block. The

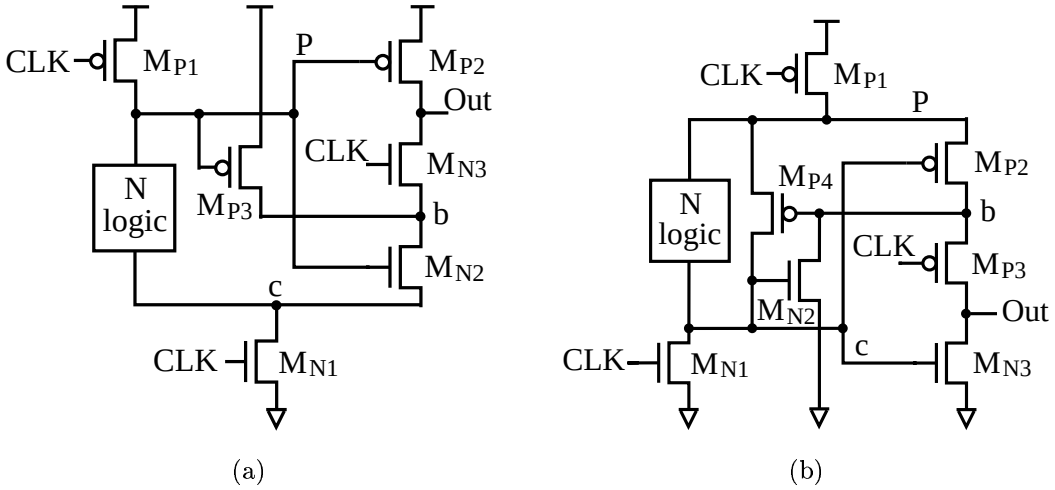


Figure 2.12: All-N-logic (ANL1) latch stages: N1-block (noninverting) (a), and N2-block (inverting) (b).

operating principle of the N2-block is as follows: When clock is high (precharge phase), NMOS transistor M_{N1} is turned ON, node c is low, NMOS transistor M_{N3} is OFF and PMOS transistor M_{P3} also is OFF. Therefore the output "OUT" is in high impedance and preserves its previous state. When the clock goes from high to low (evaluation phase), both PMOS M_{P1} and M_{P3} are ON, node P is charged to a high logic level. If the PDN is ON, node "c" is charged high and the output "OUT" discharges through M_{N3}. If the PDN is OFF, node "c" remains in a low level and the output charges to a high level. The problem in the N2-block is that when the PDN is high and the clock is low, node "c" does not reach V_{DD}. Using the positive feedback PMOS M_{P4} to make node "c" quickly rise to V_{DD} solves the problem. NMOS transistor M_{N3} avoids the charge redistribution problem as in the N1-block. This dynamic logic reaches high clock frequency by avoiding the use of the low-speed P-logic blocks.

2.3 Conclusions

In this chapter a review of the main static an dynamic CMOS logic styles was presented. Static CMOS logic combines dual pull-up and pull-down networks where only one network is activated by the inputs at quiescent state. Thus a great amount of area is wasted to implement complex logic circuits. Furthermore, the increased input load makes static CMOS slower than dynamic

logic. Static logic has higher noise margins than dynamic logic. Hence, it is less sensitive to signal integrity problems and it is suitable for systems where performance is not of interest.

The main advantage of dynamic logics is their great performance but they require careful design to ensure a reliable operation. The operation of dynamic logic is based on charge storing on a capacitive node and the input dependent discharging of that node. Dynamic logic is faster than the static counterpart due to the pull-up network suppression. Domino, TSPC and ANL use a single clock phase, hence, races are avoided and performance is increased. Domino logic can not manage inverted signals but, as TSPC logic, it is widely used in microprocessor design. TSPC logic is fast but it is limited by the P-block. ANL overcomes this problem and is suitable for high-speed circuits. In general, dynamic logic trades-off noise tolerance and performance. Thus, circuit techniques which improve the dynamic circuit noise tolerance with minimum performance degradation are required.

Chapter 3
NOISE TOLERANCE OF DYNAMIC DIGITAL CIRCUITS

In this chapter basic concepts regarding noise will be reviewed. To understand in a better way the noise problem, noise tolerance concept is explained. It will be shown the need for a dynamic noise tolerance metric and the effects of noise pulses in digital logic. A reviewing of existing noise metrics and noise tolerant techniques is made.

3.1 Preliminary Concepts

3.1.1 Noise Tolerance

Noise is defined as any disturbance that causes the voltage of an evaluation node to deviate from the nominal supply or ground rails when it should otherwise have a stable high or low level as determined by the logic and delay of the circuit [48].

As pointed out in chapter 1, there are a number of noise sources in digital circuits that affect the signal integrity, namely capacitive coupling at interconnection lines or crosstalk, inductive interconnection effects, simultaneous switching noise or ground bounce, substrate noise, resistive drops and charge sharing. According to Lohstroh [49], interconnection noise in digital circuits can be divided into three basic noise sources: series-voltage noise between gates, parallel-current noise to inputs of gates and ground bounce. Series-voltage noise may be induced by inductive coupling, parallel-current noise may be injected by capacitive coupling into

the circuit, crosstalk corresponds to this type of noise, ground bounce is a class of series-voltage noise and is induced into the supply and ground lines.

Signal integrity can be disrupted by all of these noise sources acting one at a time or together. In this thesis we devote our analysis to noise produced by adjacent interconnection lines. This noise can be due to the coupling capacitances and to the magnetic field surrounding the line of interest.

The ability of logic circuits to avoid the voltage of an evaluation node to deviate from the nominal supply or ground rails in the presence of noise is called **noise tolerance**. When the noise pulse appears in the input of a receiver gate, the noise tolerance is called noise immunity [50].

Static noise immunity, also called static noise margin, is referred to as the maximum dc voltage offset that can be withstood at the input of a logic circuit [49] [51]. In this case the noise is considered to have an infinite width and only its amplitude is of interest.

Noise margin is specified in terms of two parameters [51]: the low noise margin, NM_L, and the high noise margin, NM_H. NM_L is defined as the difference between the maximum low input voltage of the driven gate and the maximum low output voltage of the driving gate. Thus

$$NM_L = |V_{ILmax} - V_{OLmax}|$$

NM_H is defined as the difference between the minimum high output voltage of the driving gate and the minimum high input voltage of the driven gate. Thus,

$$NM_H = |V_{OHmin} - V_{IHmin}|$$

Fig. 3.1 shows graphically these definitions.

The high-gain restoring logic gates such as the static inverter, have a very nonlinear voltage transfer characteristic, Fig. 3.2. This fact gives to CMOS digital circuits an inherent noise tolerance. As long as the noise amplitude is lower than V_{IL} or falls between V_{IH} and V_{DD} on the input of a logic gate, is attenuated when propagated to the output. Nevertheless, if noise amplitude falls in the high-gain region –between V_{IL} and V_{IH}–, noise at the input will be amplified to the output. This can produce a logic failure.

Static noise margin is a metric that accounts for the noise immunity of the gates against dc voltage offsets on the input nodes. These dc voltage offsets can be due to leakage currents

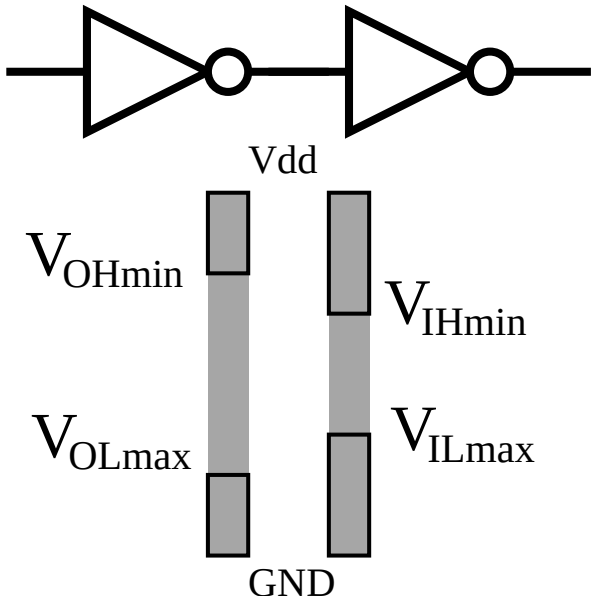


Figure 3.1: Noise margin definitions.

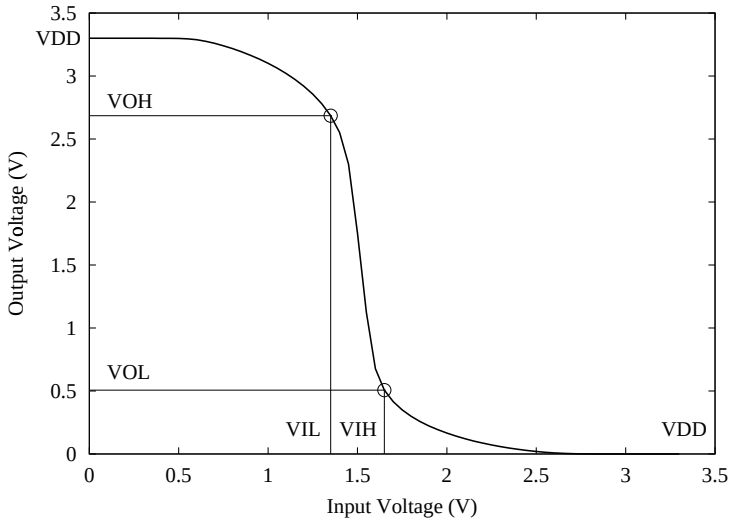


Figure 3.2: The inverter voltage transfer characteristic is very nonlinear and thus the inherent noise tolerance.

and RI noise on power supply lines. However noise disturbances can appear not only as dc offsets but in the form of pulses, as occur in capacitive coupling noise or crosstalk. So, due to the finite time response of the logic circuits a noise pulse needs more amplitude to cause a logic failure than the aforementioned dc voltage offsets. Hence, the static noise margins are a worst case metric. Accordingly, the concept of dynamic noise immunity is more general because takes into account not only the amplitude of the noise waveform but the width.

As the width of noise pulses becomes narrow the noise immunity of affected gates increases. For wide noise pulses the noise immunity tends to decrease until the situation becomes quasi-static and the noise tolerance is determined by the low noise margin. Consequently, static noise margins are a special case of dynamic noise immunity (when the width of the noise pulse is infinite). In the next section the concept of dynamic noise immunity is represented in a noise immunity curve.

3.2 Metrics for Noise Immunity and Performance

To quantify the noise immunity and performance of the noise-tolerance techniques described in this thesis different metrics and considerations are used. Three design factors are of interest:

1. Noise immunity,
2. Average power dissipation,
3. clock-output (CLK-Q) delay.

The different metrics used through this work are described below.

3.2.1 Noise Immunity Curve

Noise pulses that affect a dynamic circuit and cause unrecoverable logic errors have sufficiently high amplitude and long width. As the amplitude and width of noise pulses decrease, their effect on dynamic circuits tends to diminish. This behavior is embodied in noise immunity curves [50]. Fig. 3.3 shows two typical noise immunity curves, where all points on and above the curve represent the amplitude (A_n) and width (W_n) of the noise pulses that cause a logic error. The points below the curve are the amplitude and width combinations that do not affect

the logic behavior of dynamic circuits. A circuit with a noise immunity curve shifted to the upper part (curve NIC_2 in Fig. 3.3) is more robust to noise than a lower curve (curve NIC_1).

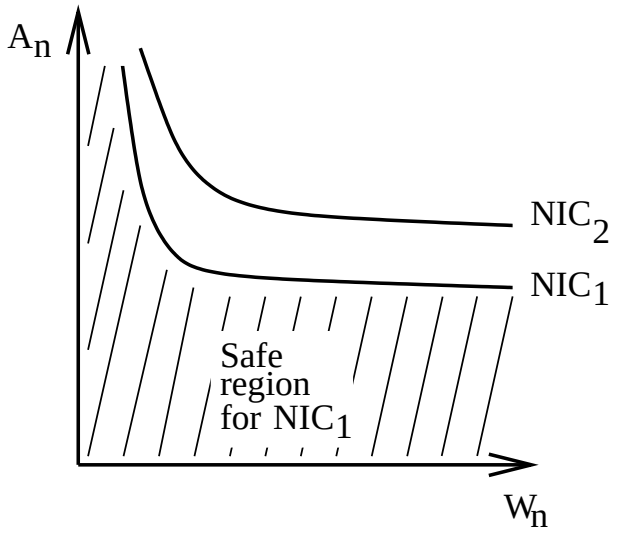


Figure 3.3: Definition of Noise Immunity Curve.

3.2.2 Average Noise Threshold Energy

The ANTE (Average Noise Threshold Energy) metric is defined as the average input noise energy that the circuit can tolerate [52]. If the input noise energy is defined as the energy dissipated in a 1Ω resistor subject to a voltage waveform with amplitude A_n and width T_n, the ANTE metric is defined as

$$ANTE = E(A_n^2 W_n) \tag{3.1}$$

where A_n and W_n are the amplitude and width of the input noise pulse, respectively, and E() is the average. Before to obtain the ANTE of a dynamic circuit, it is necessary to get its noise immunity curve. From each point in the noise immunity curve the corresponding amplitude and width are obtained and included in (3.1). Fig. 3.4 shows a noise immunity curve formed by points that correspond to noise amplitude and width pairs (A_n, W_n). These pairs are used in (3.1) in the following form to get the corresponding ANTE metric:

$$ANTE = \frac{A_1^2 \cdot W_1 + A_2^2 \cdot W_2 + A_3^2 \cdot W_3 + A_4^2 \cdot W_4 + \cdots + A_m^2 \cdot W_m}{m} \tag{3.2}$$

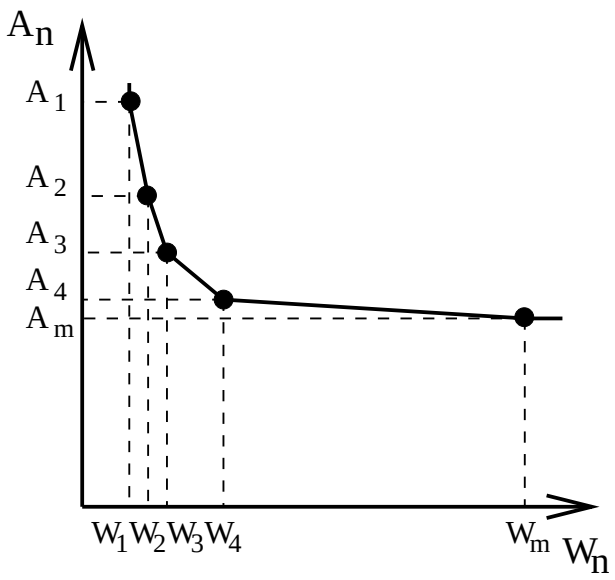


Figure 3.4: The ANTE metric is obtained from a noise immunity curve.

A higher ANTE metric implies that more noise pulse energy is needed to discharge the dynamic node and generate a logic failure.

3.2.3 Unity Noise Gain

Unity Noise Gain (UNG) is defined as the amplitude of input noise A_n that causes an equal-amplitude noise pulse at the output voltage V_{out} [53], i.e.,

$$UNG = \{A_n : A_n = V_{out}\} \tag{3.3}$$

UNG is easy to obtain in a circuit simulator like SPICE. However, it only accounts for noise amplitude, and for the deep submicron era, the width of the noise must be taken into account. So, UNG is only the best choice for a rapid analysis of noise immunity.

3.2.4 Power Metric

The average power consumption of the circuits under test was measured using the power meter proposed in [54]. The power consumption was measured in several clock cycles and then divided between the number of clock cycles to have the average power consumption per clock cycle.

Fig. 3.5 shows the power meter. Basically this circuit integrates the current delivered by the voltage supply (i_{dd}) in a variable time period determined by V_{SW}. With a correct selection of β, ($\beta = C_1 V_{dd}/T$, where T is the clock period), the capacitor voltage V_C will reflect the average power dissipated.

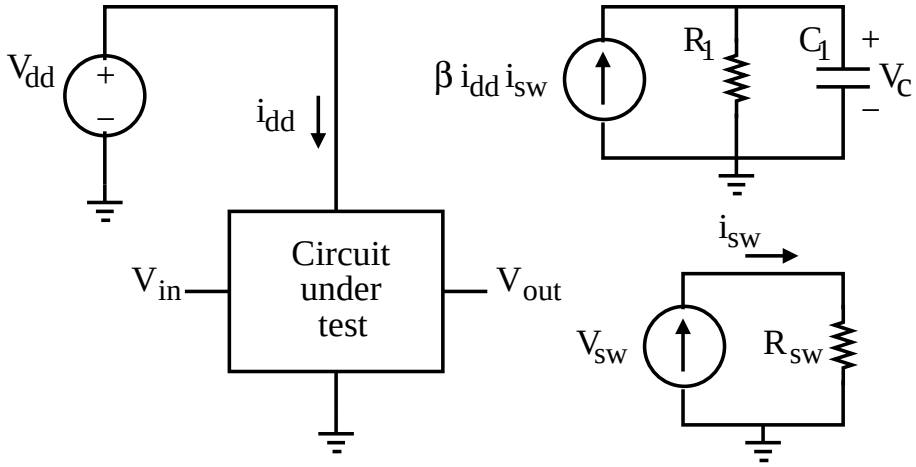


Figure 3.5: Power meter for SPICE simulations.

3.2.5 Delay Metric

In this thesis delay is measured as the time difference between 50% points of rising clock edge and rising output edge, assuming that the input signal has been set early enough relative to the rising edge of the clock signal [55]. Dynamic digital circuits like TSPC or Domino are designed to have a fast rising transition at the output because this is the critical transition. These circuits are referred as *skewed-evaluate* circuits [56]. Because this, we measure the delay in that way.

3.3 Noise Effects on Dynamic Digital Logic

In precharged dynamic circuits like TSPC and Domino, dynamic evaluation nodes are susceptible to crosstalk especially during the part of normal system operation where they are not connected to the power supply or ground. Pipelined TSPC circuits suffer twice this problem. The output nodes of the N-block or P-block are not connected to the power rails during precharge phase (see Fig. 3.6). Furthermore, whether the logic function is not in ON state in evaluation phase

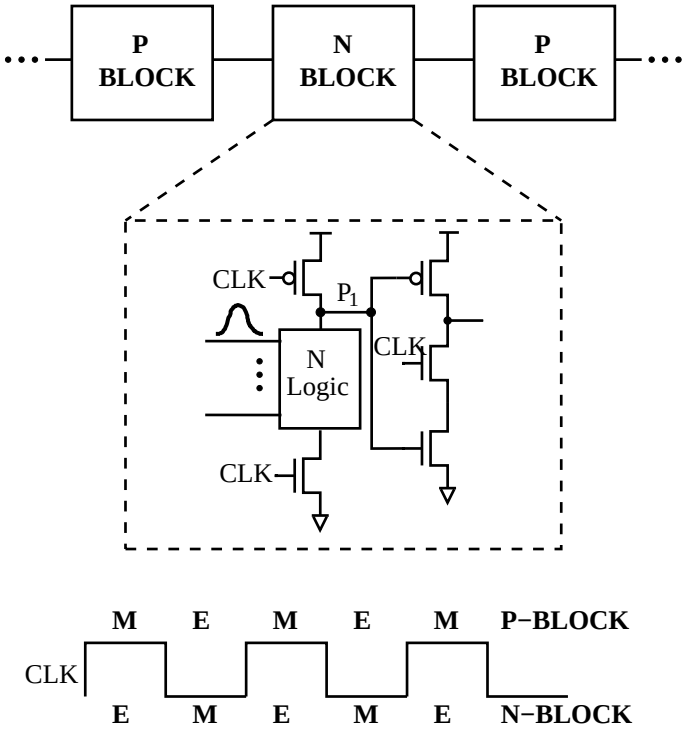


Figure 3.6: A general schematic of pipelined precharged logic circuits.

(E), internal dynamic precharge nodes of both blocks will not be connected to the power rails.

While clock remains low N-blocks are in precharge phase and their inputs take a new value or remain unchanged. When clock goes high N-blocks enter in evaluate phase. Let's assume all inputs of an N-block remain high except the upper one which goes low (see Fig. 3.6). When a noise pulse is generated at the top input of the N-block the internal dynamic precharge node P_1 can have a direct path to ground if noise amplitude is greater than V_t which is the threshold voltage of the NMOS transistor controlled by the noisy input in the N-logic. Consequently, P_1 is discharged as far as the noise amplitude is greater than V_t. Fig. 3.7 shows how in a TSPC AND gate the noisy input discharges the dynamic precharge node P_1 and the output node has an undesirable logic transition from low to high. Furthermore, the glitches also increase the power consumption. In this way, digital noise effects may degrade the performance and reliability of the circuit. These deleterious effects are more evident in submicron technologies.

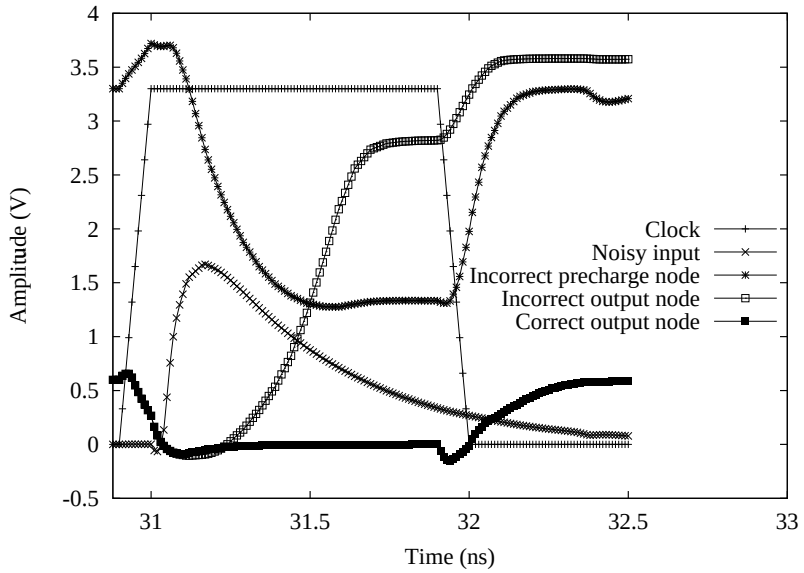


Figure 3.7: Noise effect on N-block output.

3.4 Previous Noise Tolerant Dynamic Digital Circuit Techniques

Rising the noise threshold voltage V_{nth} of the gate is one effective way to increase the noise tolerance of digital gates, where V_{nth} is defined as the minimum input voltage required to cause a logic transition at the output. Most of the noise-tolerant techniques rise V_{th} by precharging the N-logic internal nodes using the input data, the internal dynamic node P_1 or the clock signal. This precharge increases the threshold voltage (V_t) of the NMOS transistors in the PDN taking advantage of the body effect. Consequently, V_{nth} is also increased. In this section a review of some recently proposed noise tolerant techniques that use these strategies is presented showing their advantages and disadvantages.

3.4.1 Inverter Technique

Fig 3.8 shows the Inverter technique applied to a 2-input domino AND gate [57]. In this technique each drain of the NMOS transistors that conform the PDN block is precharged by the input data through PMOS pull-up transistors. The increased noise tolerance is due to the body effect. This technique can be applied for the design of AND/NAND gates. However, it

cannot be used for dynamic OR/NOR gates since some combinations will cause static power dissipation. This technique has the disadvantage that each input is loaded by an extra PMOS

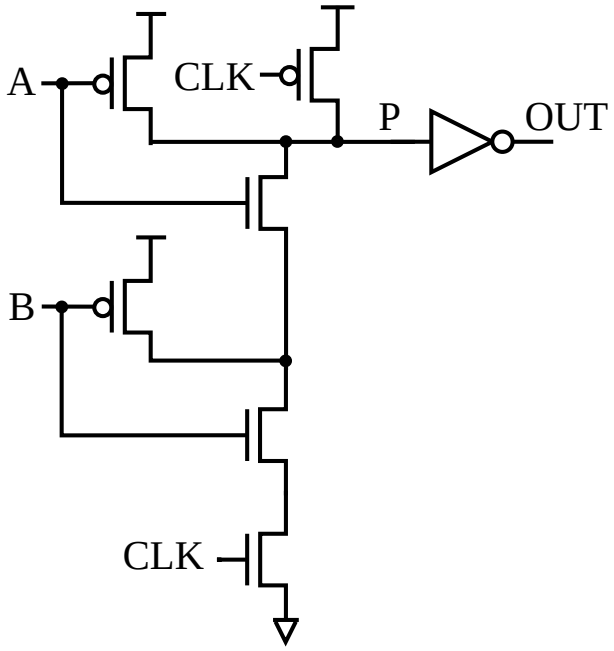


Figure 3.8: 2 input domino AND gate using Inverter technique.

transistor and a bigger driver is required. Additionally, the inverter-like operation slow down the evaluation of the precharge node P.

3.4.2 Selective Pull-up Technique

The Selective Pull-up (SP) technique [58] is a generalization of the Inverter technique and can be applied to any gate.

To apply this technique first all the branches in the PDN block must be identified. Then a pull-up network formed of a stack of series PMOS transistors is connected to the common (NMOS) drain of the branches. A PMOS transistor is added for each NMOS transistor in the branches. The gate of each PMOS transistor is connected to the corresponding NMOS transistor.

Fig 3.9 shows the SP technique applied to an AOI gate. As seen, the PDN is formed by two branches and one of them has two series transistors. In the common drain of both branches

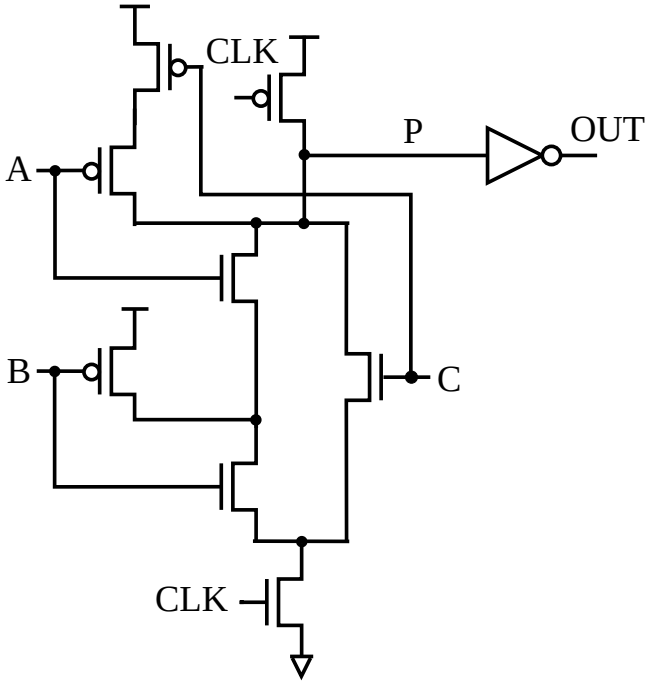


Figure 3.9: Selective Pull-up technique implemented in a 2 input domino AND gate.

two stacked PMOS transistors are connected and their gates are connected to the corresponding gates of the NMOS transistors. The third NMOS transistor has a pull-up PMOS transistor as in the Inverter technique.

This technique has the disadvantage that each input is loaded by an extra PMOS transistor and a bigger driver is required. Additionally, the inverter-like operation slow down the evaluation of the precharge node.

3.4.3 PMOS Pull-Up Technique

Fig. 3.10 shows a 2 input AND gate using PMOS Pull-Up technique [59]. In this technique a PMOS transistor M_P is added. In evaluation phase (CLK="0") the transistor M_{N1} is turned ON and starts to discharge the node P_1, which is the source of transistor M_{N2}. As the voltage at node P_1 drops, the transistor M_P turns ON and forms a resistive voltage divider. The voltage at node P_1 increases and rises the threshold voltage of the transistor M_{N2} due to body effect. In this way, the transistor M_{N2} will turn ON only when the difference between the input voltage

at B and the source voltage at node P_1 exceeds the raised threshold voltage of the transistor.

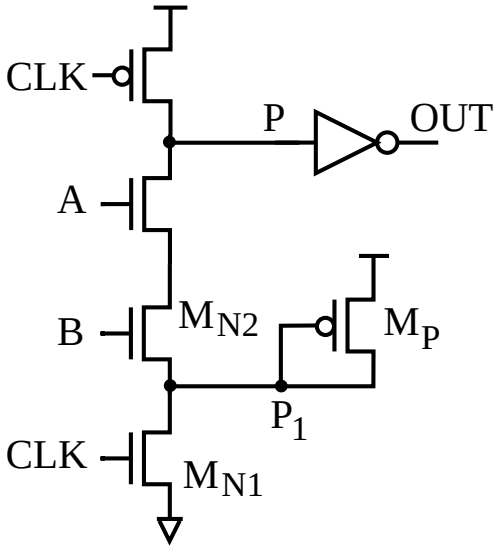


Figure 3.10: 2 input domino AND gate using PMOS Pull-Up technique.

This technique has some disadvantages. In evaluation phase, if the PDN is on, the dynamic precharge node can only be greater than the node P_1 voltage. Consequently, the output driver will have leakage current and the output may not make a full rail transition. In addition, there is static power dissipation due to the ON transistors M_{N1} and M_P. To alleviate these problems, the transistor M_{N1} can be sized up, which will reduce the node P_1 voltage. But reducing P_1 voltage also decreases the noise tolerance of the technique.

3.4.4 Mirror Technique

The mirror technique [60] shown in Fig. 3.11 for a 2 input AND gate duplicates the N-logic and the node between the bottom and top N-logic is precharged through transistor M_n employing the principle of a Schmitt trigger. In the memory phase the transistor M_n is ON and the node N_P is precharged to $V_{dd} - V_{t,M_n}$. Due to body-effect the noise threshold voltage of the top N-logic is increased. A resistive voltage divider is formed between the transistor M_n and the bottom N-logic if during evaluate phase all inputs rise. The bottom N-logic pulls-down the node N_P and the top N-logic turns ON to discharge the dynamic evaluation node. Besides this technique does not suffer from static power dissipation, adds a delay penalty due to the

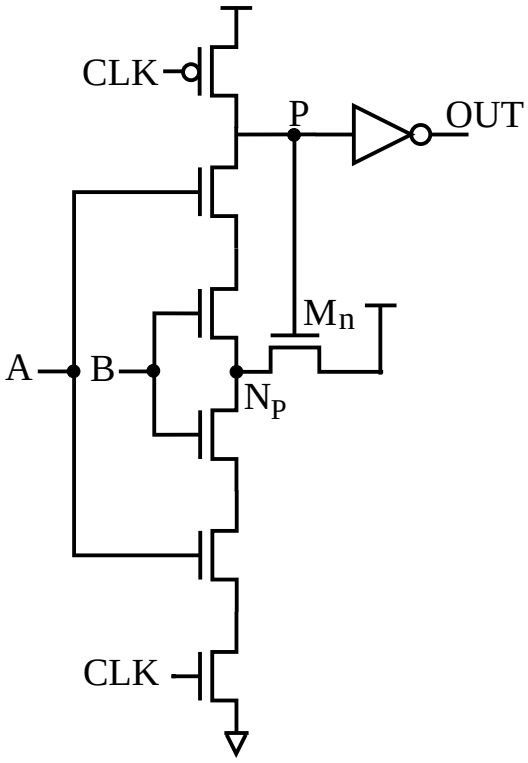


Figure 3.11: Mirror technique implemented in a 2 input domino AND gate.

duplicated N-logic and the increased capacitance in the internal dynamic node due to transistor M_n.

3.4.5 Bobba's Technique

Fig. 3.12 shows Bobba's technique [61] for a 2 input AND gate. In this technique more transistors are added to the N-logic to improve the noise-tolerance. One NMOS transistor is added in the N-logic per each NMOS transistor in the original N-logic and a PMOS transistor rises the nodes N_1 and N_2 to V_{DD} while gate inputs are low. If during evaluate phase all inputs go high a voltage divider is formed by PMOS and NMOS added transistors at nodes N_1 and N_2. The improved noise tolerance is obtained by two ways: (a) the V_{th} of the AND gate equals to V_{th} of the static inverters that operate as voltage dividers, V_{th} can be adjusted modifying the transistor width to length ratios; and (b) by rising the source node voltage of the top NMOS in the N-logic avoids sub-threshold leakage current from drain to source. One drawback of this

technique is the significant delay penalty for AND gates due to the duplicated N-logic and the increased capacitance at the gate inputs. Power consumption penalty is increased because two transistors are added per each transistor in the N-logic and if internal nodes are discharged the precharge rises from ground to V_{DD}.

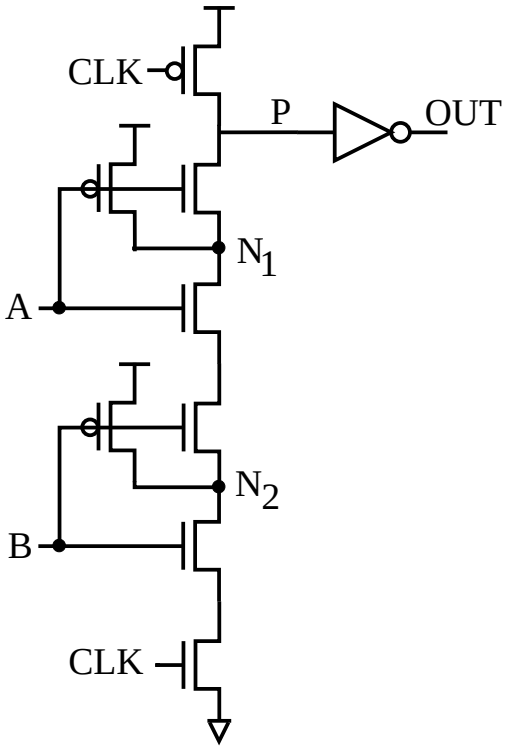


Figure 3.12: Bobba's technique implemented in a 2 input domino AND gate.

3.4.6 Twin-Transistor Technique

The Twin-Transistor technique [62] shown in Fig. 3.13 rises the voltage of the N-logic internal nodes via additional transistors M_{TT}. Due to body-effect the noise threshold voltage of the N-logic transistors pulls-up. Hence, the tolerance of the gate improves. One drawback of this technique is that using gate inputs to rise the voltage of the N-logic internal nodes adds load capacitances to the drivers of the gate inputs. Furthermore, this technique cannot be applied to pipelined logic like TSPC because N-block inputs are floating in evaluation phase. Consider the case when this technique is applied to N-blocks in a pipelined system (like that of Fig. 3.6). If

all inputs of an N-block are high at the beginning of the evaluation phase, the voltage level of the upper input is degraded by a charge redistribution mechanism. The charge redistribution path is indicated with a dotted line in Fig. 3.13. In this way, to apply the Twin-transistor technique in TSPC logic it is necessary to place buffers between N- and P-blocks.

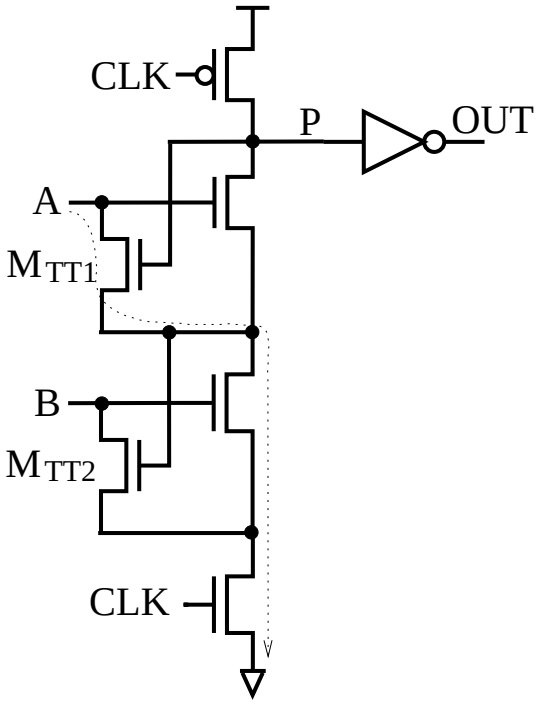


Figure 3.13: Twin-transistor technique implemented in a 2 input domino AND gate.

3.4.7 Input Controlled Refresh (ICR) Technique

The Input Controlled Refresh (ICR) [63] shown in Fig. 3.14 for a 2-input domino AND gate, has the property of recover the logic level after a noise pulse appears. This technique requires a complementary PMOS network. In precharge phase both PMOS transistors M_{P1} and M_{P2} are ON. This precharges the dynamic precharge node and the gate of the keeper transistor to a high logic level. Consequently, the keeper is OFF. If the inputs are LOW, the refresh circuitry (PMOS transistors M_{P3} and M_{P4}) is ON and the node P_2 is also precharged HIGH.

During evaluation phase, if both inputs go HIGH the refresh circuitry is cut off because PMOS transistors M_{P3} and M_{P4} are OFF. Because this the dynamic precharge node discharges

without any resistance from the keeper transistor. When any one of the inputs remains LOW, at least one of the PMOS transistors in the refresh circuitry is turned ON. This discharges the gate node of the keeper transistor and the precharge node is holding HIGH.

If a noise pulse appears during evaluation phase the precharge node can be discharged if the noise pulse has enough energy. Nevertheless, the precharge node recovers the logic level after the noise pulse disappears since at least one PMOS transistor returns to a LOW logic state and the keeper is turned ON again.

The refresh property is the main advantage of this technique. Drawbacks of this technique are the glitches caused by noise pulses that consume power. The extra load at the inputs forces the drivers to have more strength. Furthermore, during the time the precharge node is discharged by a noise pulse, the output may switch and a false logic state can be propagated.

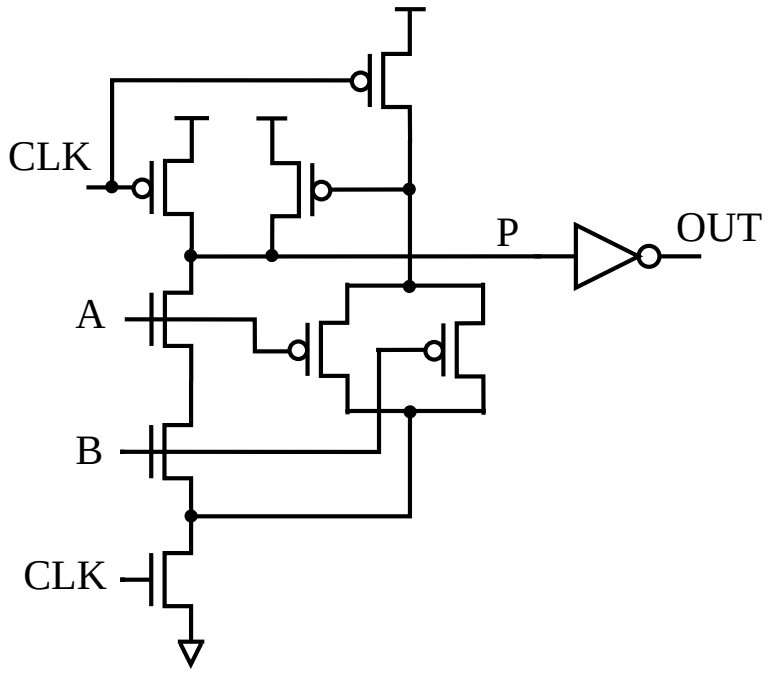


Figure 3.14: Input Controlled Refresh (ICR) technique implemented in a 2 input domino AND gate.

3.4.8 Clock as Shield (CASh) Design Methodology

Clock as Shield (CASh) [64] is a layout methodology to reduce crosstalk noise effects in domino circuits. In this methodology clock interconnections are used as shielding wires to reduce the peak voltage in a capacitive coupled victim input. Fig. 3.15 shows this idea in a 2-input Domino AND gate. Since CASh methodology is a layout methodology, speed penalty and area overhead can be avoided.

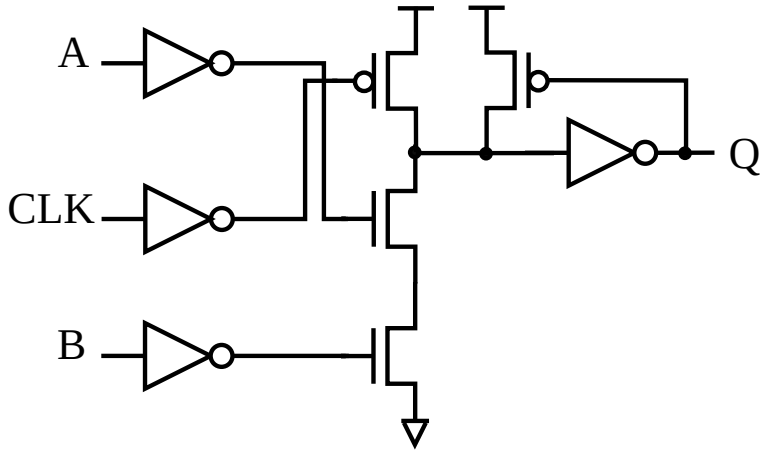


Figure 3.15: Clock as Shield (CASh) technique implemented in a 2 input domino AND gate.

3.5 Conclusions

The fundamental concepts on digital noise have been described. Static and dynamic noise margins concepts are fundamental to understand the signal integrity problem. Static noise margins have traditionally been used to describe the ability of logic circuits to avoid the voltage of an evaluation node to deviate from the nominal supply or ground rails in the presence of noise. However, due to the finite time response and the low pass filter behavior of the logic gates a noise pulse with an amplitude higher than the static noise margins of a gate can be tolerated by that gate. In this way, static noise margin becomes an obsolete metric. Dynamic noise margin better describes the noise tolerance of a circuit because it accounts for pulsed noise sources. Static noise margin is a pessimistic metric and is a subset of dynamic noise margin.

Metrics for noise immunity and performance are reviewed. Noise Immunity Curve, ANTE,

and UNG are the used metrics for noise immunity. Noise Immunity Curves enclose the tolerance of the gates over amplitude and width combinations of noise pulses. Unfortunately, when comparing two noise tolerance curves that overlap each other the reading becomes a difficult task. ANTE metric solves this situation and gives a quantitative noise tolerant metric. UNG do not take into account the width of the noise pulse but it can be obtained relatively fast. Thus, UNG is desirable for a rapid estimation of the noise tolerance of a circuit.

The effects of a crosstalk noise pulse at the input of a dynamic gate in a pipeline system are analyzed. Due to the charge storing behavior of dynamic nodes that noise pulses degrade the reliability of dynamic circuits. When a noise pulse generates an undesirable logic transition in a dynamic logic gate, the output can not recover the correct logic state and the error can be propagated causing performance degradation.

Finally, some of the recent published noise tolerance techniques are presented and their advantages and drawbacks are commented. In general, noise tolerant circuit techniques increase the noise threshold of the gate by increasing the threshold voltage of the NMOS transistors in the pull down network due to body effect. CASh [64] and Logic-Aware Layout Methodology (LALM) [65] [66], recently published, which reconfigures transistors and reorders nets considering the circuit functionality to enhance noise immunity, are new layout methodologies to improve noise immunity. These kind of methodologies are not in the scope of this work.

Chapter 4
A NEW NOISE TOLERANT DYNAMIC CIRCUIT TECHNIQUE

In Chapter 3 the previous noise tolerance dynamic circuit techniques were reviewed. Although these techniques rise the dynamic digital circuits noise tolerance they show some limitations. The main limitation is their lack of flexibility, i.e., these techniques are limited to some logic styles or some Pull Down Network (PDN) logic structures. The most used logic for applying the previously proposed noise tolerant techniques is domino logic. Besides, previously proposed noise tolerant techniques increase the input load capacitance due to the additional precharge transistors, as a result, dynamic logic loses one important advantage over static logic.

Hence, there is a need for a flexible noise tolerant technique that increases the noise immunity for different dynamic logic styles with a slight performance penalty.

In this chapter a new noise tolerant dynamic circuit technique [67] [68] [69] is introduced. The operation of this new noise tolerant technique is analyzed as well as its performance in TSPC and Domino gates. The main objective is to increase the noise immunity of dynamic digital circuits with a slight performance penalty.

4.1 Proposed Technique Structure Applied to TSPC Logic

Due to timing requirements in computer systems high performance pipelined circuits are widely used nowadays. The TSPC logic style is an attractive design technique to implement pipelined circuits but, as noted in Chapter 3, it has low noise immunity.

4.1.1 Structure of the Proposed Technique

Fig. 4.1(a) shows a general conventional TSPC precharge latch. The pull-down network can be a simple transistor or AND-OR input combinations. In this way, a variety of logic functions can be formed. The dynamic precharge node (P_1) is indicated. To implement the proposed noise tolerant technique three steps must be followed:

1. The first step is to insert an NMOS transistor (M_N) between the precharge P_1 node and the PDN, see Fig. 4.1(b). An additional node (P_2) appears.

2. Next, an inverter delay circuitry is placed to locally generate the NCLK signal from the clock (CLK) to control the gate of the transistor M_N, see Fig. 4.1(c).

3. Finally, a PMOS transistor (M_P) is added between the node NCLK and the P_2 node, see Fig. 4.1(d).

Note that in Fig. 4.1(d) the PDN has not been modified, i. e., the inputs have not been used to precharge any internal node in the PDN. This is advantageous because the capacitive loads at the inputs remain the same and there is no need to resize the input drivers.

4.1.2 Operation of the Proposed Technique

The proposed noise tolerant technique is explained with the help of Fig. 4.2(a). A timing diagram showing the different operation stages of the proposed technique is shown in Fig. 4.2(b).

On the falling edge of the clock signal (CLK) the circuit enters in the precharge phase, [stage I in Fig. 4.2(b)]. The dynamic P_1 node is precharged to a HIGH logic level, and the output OUT is isolated from the inputs holding its previous value. As noted in Fig. 4.2(b), the NCLK signal is in a LOW logic state in stage I. Consequently, the transistor M_N is OFF and the transistor M_P is turned ON. A delay time after the beginning of the precharge phase the NCLK signal rises to HIGH [stage II in Fig. 4.2(b)] turning ON the transistor M_N. The P_2 node is precharged to V_{DD} thorough M_P. On the rising edge of the clock, the circuit enters the evaluation phase. Here, two stages are distinguished. In stage III, the circuit is in the transparent mode and a *transparency window* is defined. The transistor M_P is turned OFF and the value of output OUT is determined by the state of the PDN. If the PDN is ON the dynamic

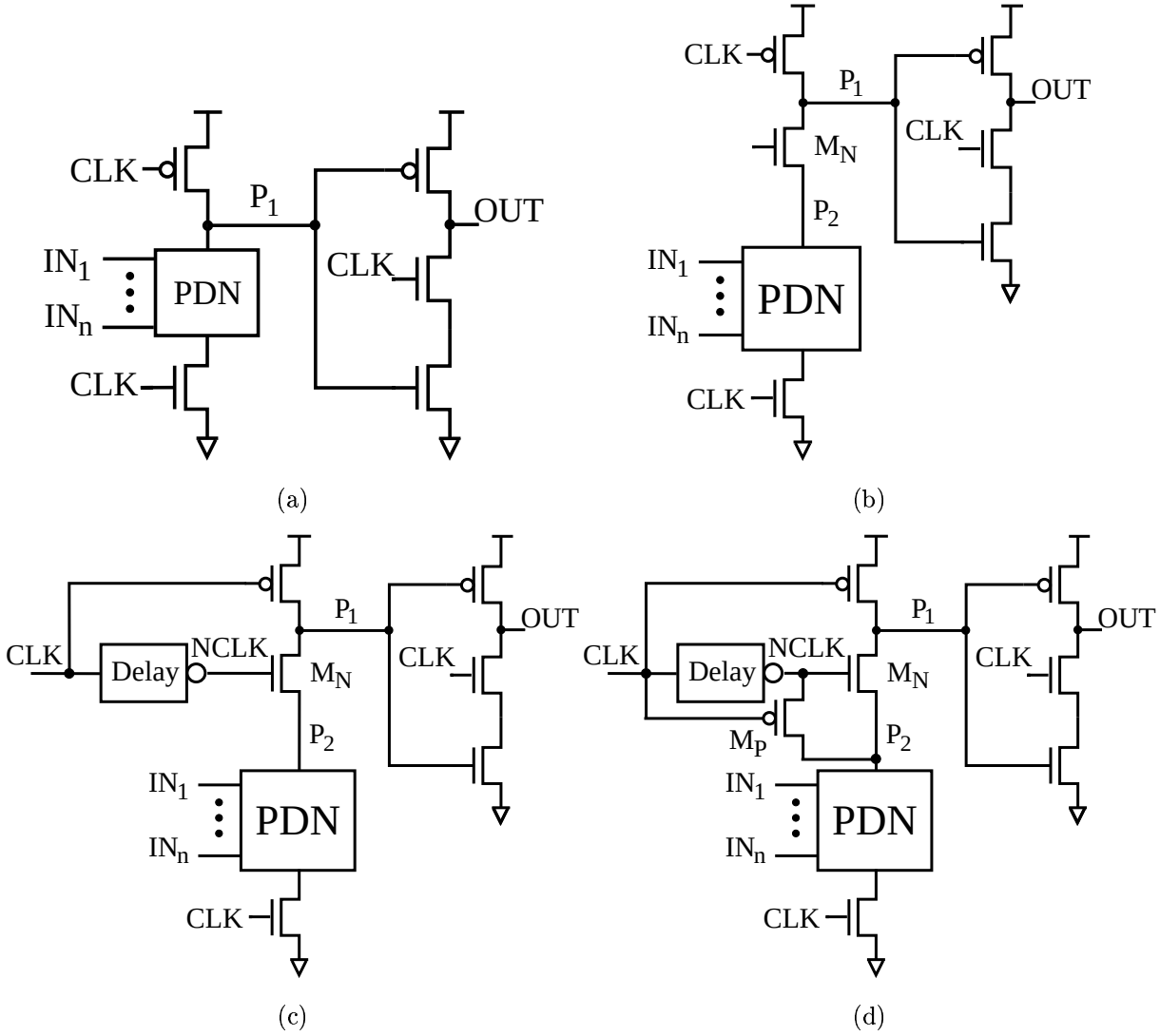


Figure 4.1: Derivation of the proposed noise tolerant technique: (a) the conventional TSPC precharge latch, (b) an NMOS transistor (M_N) is inserted between the precharge P_1 node and the PDN, (c) an inverter delay circuitry locally generate the NCLK signal from the clock signal (CLK) to control the gate of the transistor M_N, and (d) a PMOS transistor (M_P) is added between the node NCLK and the P_2 node.

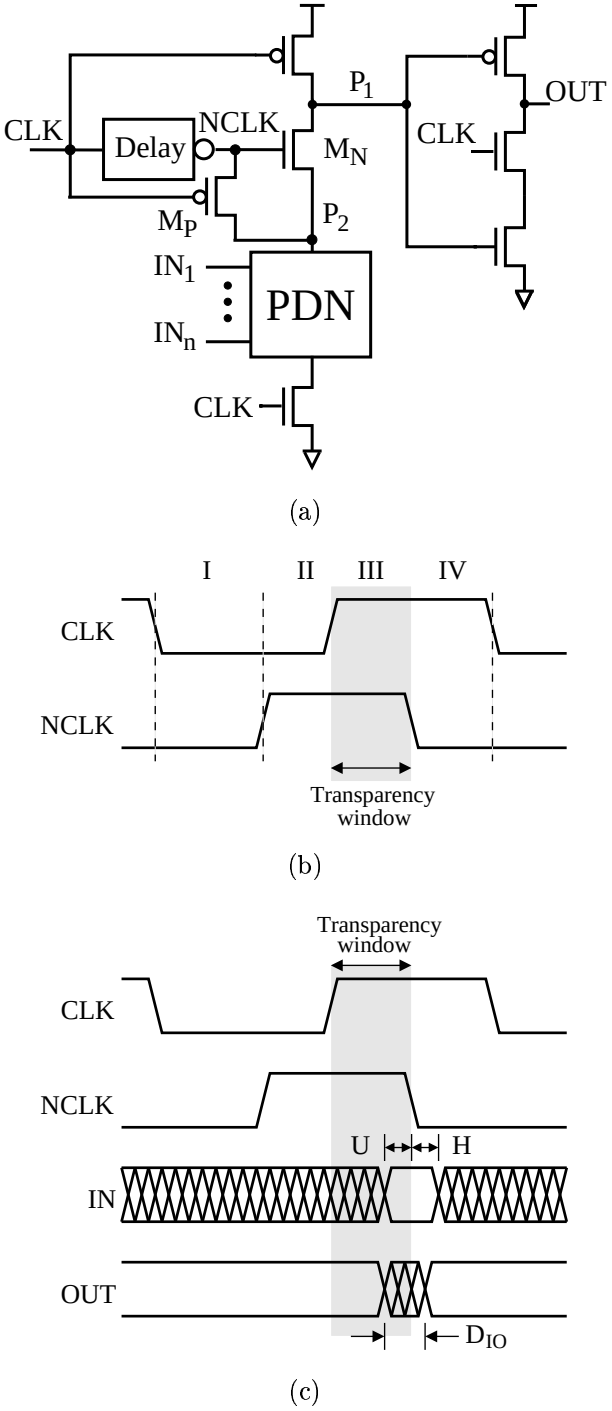


Figure 4.2: (a) General schematic of the proposed noise-tolerant dynamic circuit technique, (b) timing diagram to explain the operation of the proposed technique, and (c) timing diagram showing the setup and hold times of the proposed technique.

P_1 node is discharged and the output OUT goes high. If the PDN is OFF no dc path to ground is formed and P_1 node remains HIGH, consequently, the output OUT goes LOW. In stage IV, NCLK goes LOW turning the transistor M_N OFF. So P_1 and OUT are isolated from the PDN during the rest of the evaluation phase because the evaluation of the PDN is disabled.

The proposed technique, when applied to TSPC latches, transforms these conventional latches in a class of hybrid latches [70]. Hybrid structures shift the reference point of setup and hold time from the rising edge of the clock to the falling edge of the NCLK signal, which is the end of the transparency window. Thus, the setup and hold times are functions of the width of the transparency window when they are measured in reference to the rising edge of the clock [55]. Fig. 4.2(c) shows the setup (U) and hold (H) times as well as the input to output delay (D_{IO}) of the proposed noise tolerant technique taking as reference the falling edge of the NCLK signal. The stable, metastable and failure regions [55] of a latch with the proposed technique are illustrated in Fig. 4.3. The point marked as optimum setup time is the data-clock (D-CLK) delay which is the limit beyond which the performance of the latch is degraded.

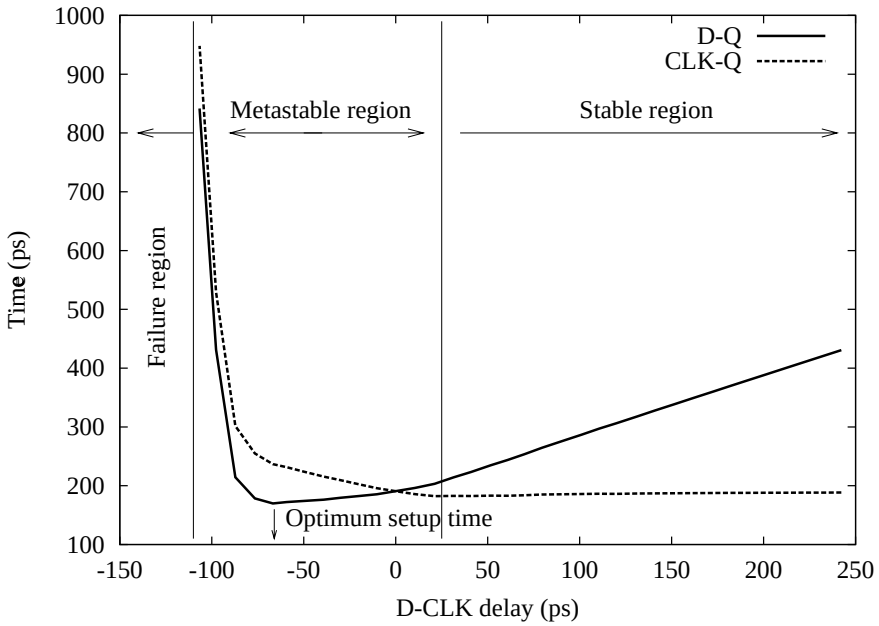


Figure 4.3: TSPC latch with proposed noise tolerant technique, stable, metastable and failure regions.

4.1.3 Noise Tolerance Mechanism of the Proposed Technique

The operation of the proposed technique is analyzed in the presence of crosstalk noise [refer to Fig. 4.2(a)]. Assume that in evaluation phase (CLK=1) all the inputs are HIGH except one in which a crosstalk pulse appears turning the PDN momentarily ON. Then a direct path from P_1 to ground is generated. Under this situation the proposed technique uses two mechanisms to increase the noise tolerance:

1. The P_2 node has already been precharged to V_{dd} prior to evaluation phase. This fact increases the threshold voltage of the transistor M_N due to body effect [51]. Consequently, the noise pulse at the inputs of the gate will require a larger amplitude to discharge the dynamic P_1 node and to generate a logic failure at the output. In this way, the noise immunity of the circuit is increased during the transparency window.

2. While evaluation phase is in process the dynamic node P_1 is isolated from the PDN because NCLK goes LOW. The noise immunity is indeed improved because any noise influence at the circuit inputs will not be reflected at the node P_1 and, hence, at the output.

To understand in a better way how the precharge of the P_2 node increases the noise immunity of the gate a first order expression for the threshold voltage taking into account the body effect will be analyzed [51]:

$$V_t = V_{t0} + \gamma \left[\sqrt{(2\phi_b + |V_{sb}|)} - \sqrt{2\phi_b} \right] \tag{4.1}$$

where V_{sb} is the substrate bias of the transistor, V_{t0} is the threshold voltage for $V_{sb} = 0$, ϕ_b is the bulk potential, and γ is a constant that describes the substrate bias effect. It is clearly noted that if the substrate bias V_{sb} were zero, the threshold voltage would reduce to V_{t0}.

Fig. 4.4 shows the voltage threshold value for several substrate-source voltages in an NMOS transistor. 0.35 μm AMS level 49 transistor parameters have been used in the analysis. As it can be seen, the threshold voltage increases as the body bias does when body effect is taken into account. Specifically, the change in threshold voltage is proportional to the root of substrate bias: $\Delta V_t \propto \gamma\sqrt{V_{sb}}$.

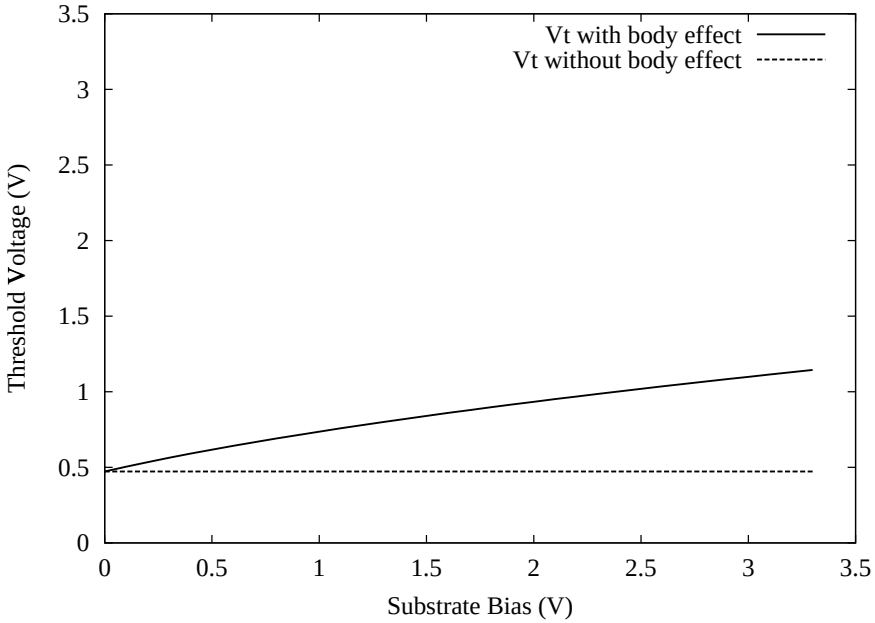


Figure 4.4: Substrate bias effect on the threshold voltage for an NMOS transistor.

4.1.4 Design Requirements of the Transparency Window

The transparency window size is the main design factor to take into account because it determines the performance and the noise tolerance level of the circuits.

The transparency window width t_{tw}, (see Fig. 4.5) is defined as

$$t_{tw} = t_D^{max} + \Delta t \tag{4.2}$$

where t_D^{max} is the discharge time of the P_1 node and Δt is the time difference between the falling voltage waveform of P_1 node and NCLK. t_D^{max} is determined by the stack of NMOS transistors formed by M_N, the PDN and the clocked transistor [see Fig. 4.2(a)]. The transparency window must be larger than the discharge time of P_1 because if not, when the PDN is ON, the precharge P_1 node will not discharge completely. Δt is defined as the extra time that the transparency window needs to assure a correct gate operation. Obviously, if Δt is very large we will be sure that the gate operates properly but at expenses of less noise immunity. Remember that during the transparency window the noise immunity comes by precharging the internal node P_2. On the other side, if Δt is very narrow, higher noise tolerance can be reached but the precharge node P_1 would not discharge completely, hence, an incorrect logic level may appear at the output.

In this way, the trade-off between noise immunity and performance is determined by the transparency window size. Furthermore, the local generation of the NCLK signal by the delay circuitry allows better control of the transparency window width, so that a sufficiently narrow transparency window can be produced and better noise tolerance can be achieved.

It is important to mention that even if Δt is narrow in such a way that P_1 does not discharge completely the output voltage can still reach a logic level "1" with a slight delay penalty, see Fig. 4.6. Hence, with a careful design of the transparency window, higher noise tolerance can be achieved.

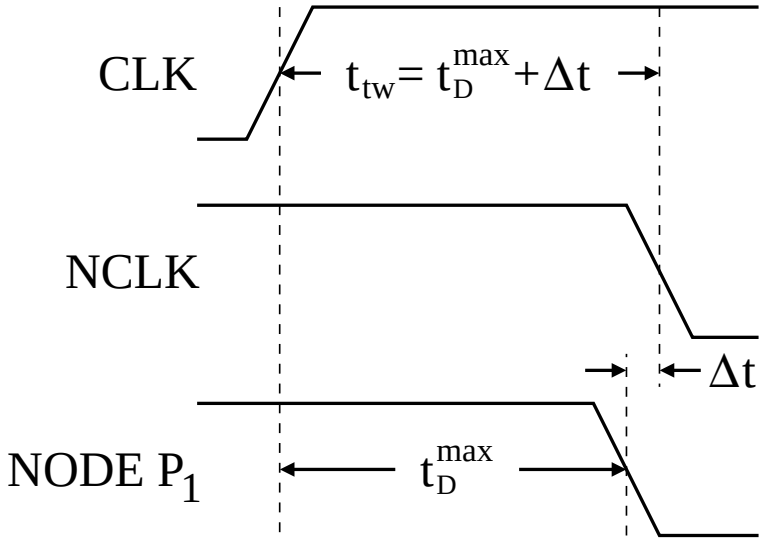


Figure 4.5: The delay time for the transparency window depends on the discharge time of the precharge P_1 node.

4.1.5 Application to a TSPC AND Gate

In the general schematic of the proposed technique [see Fig. 4.2(a)], the PDN is replaced by any combination of NMOS transistors to implement the desired logic function embedded in the latch. A 2-input AND gate is formed by replacing the PDN of Fig. 4.2(a) by two series transistors, as shown in Fig. 4.7. HSPICE simulations were done at a clock frequency of f_{CLK}=1 GHz and a voltage supply of V_{DD}=3.3 V.

The delay circuitry can be constructed with three cascaded static inverters [see Fig. 4.7]. By a proper selection of the size of the inverters in the delay circuitry the width of the

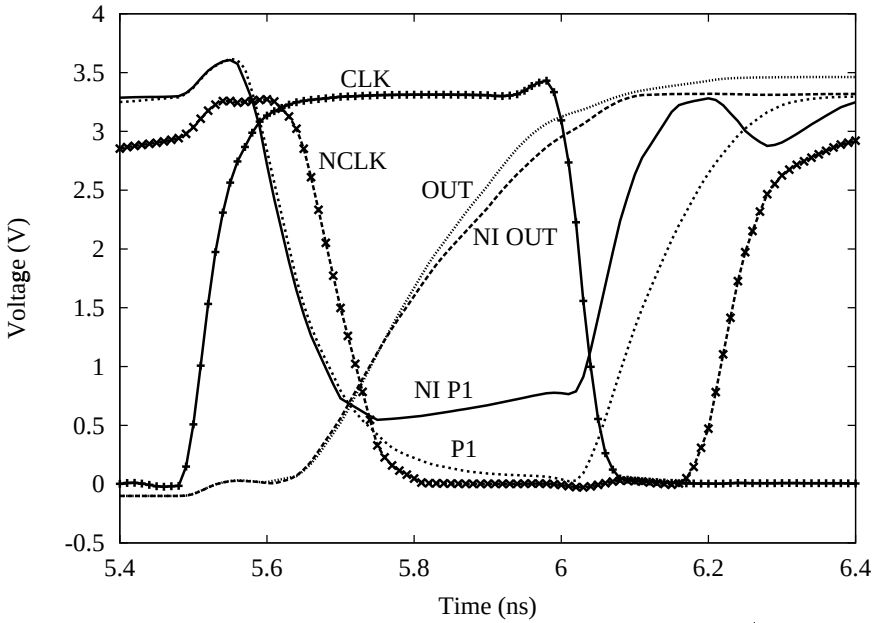


Figure 4.6: Transient response of two 4-input OR gates. Waveforms P1 (precharge node) and OUT (output node) correspond to a conventional gate. NI P1 and NI OUT correspond to the Noise Immune (NI) gate implemented with the proposed technique. The node marked as NI P1 is not completely discharged, however, the output (NI OUT) reaches a HIGH logic level.

transparency window can be adjusted to meet the noise immunity-performance requirements. Fig. 4.8 shows the HSPICE simulation of the noise tolerant AND gate.

Shortcomings of the proposed technique are referred to charge sharing. Fig. 4.9 shows a transient analysis where the clock (CLK) and NCLK signals are shown as well as the waveforms of the nodes P_1 and P_2 [see Fig. 4.7]. Two charge redistribution problems are identified:

1. First, if both NCLK and voltage at P_2 node are low at the beginning of evaluation phase, M_N will be OFF because its gate to source voltage V_{gs} is zero. When NCLK goes HIGH, M_P starts to precharge the P_2 node. P_2 is not precharged immediately due to the finite response time of M_P. So, M_N turns ON before the P_2 node can be precharged to V_{dd}. In this way, charge redistribution between P_1 and P_2 occurs. This charge redistribution generates a glitch at P_1 node (see Fig. 4.9 at approximately 4.2 ns). As the voltage at P_2 node continues rising, the gate-source voltage of M_N decreases and M_N is finally turned OFF.

2. Second, when both CLK and NCLK are low at the beginning of the precharge phase a

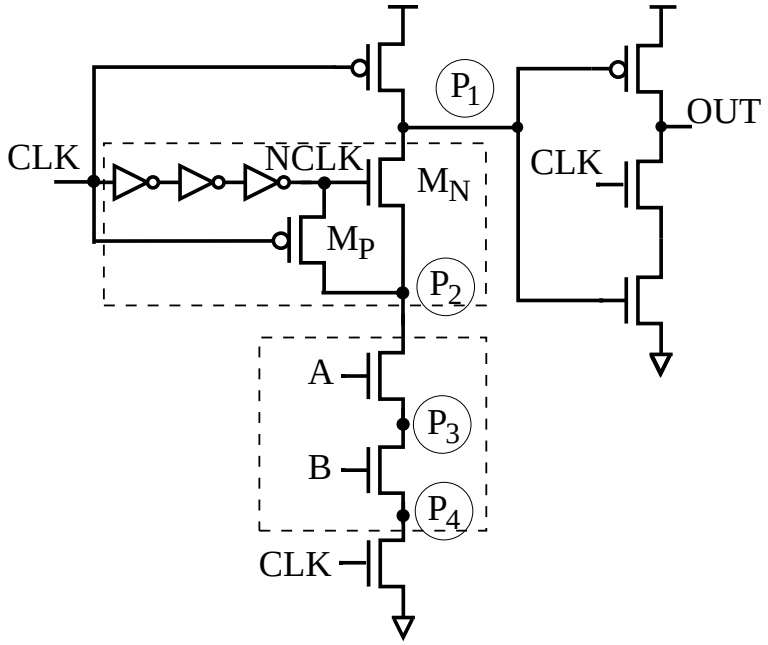


Figure 4.7: 2-input AND gate with the proposed noise-tolerant dynamic circuit technique.

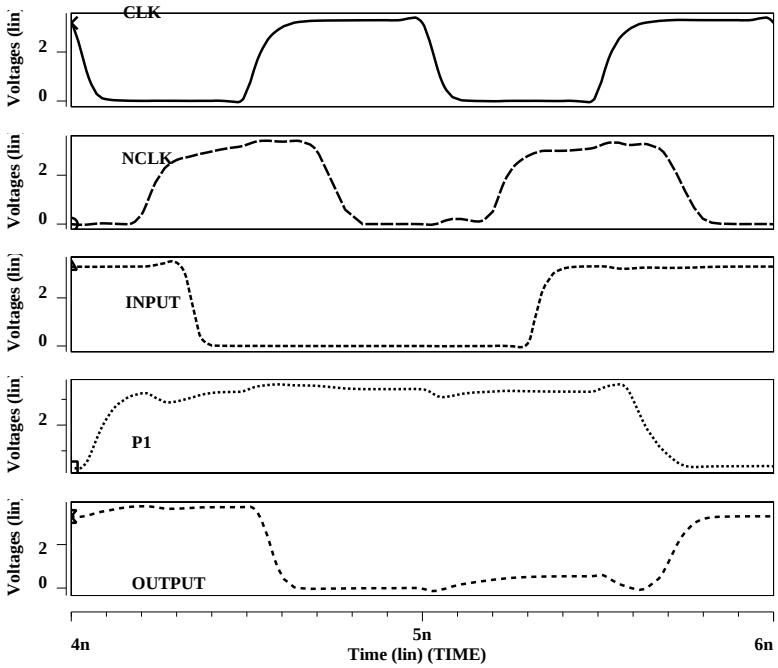


Figure 4.8: A transient analysis of a 2-input AND gate implemented with the proposed technique.

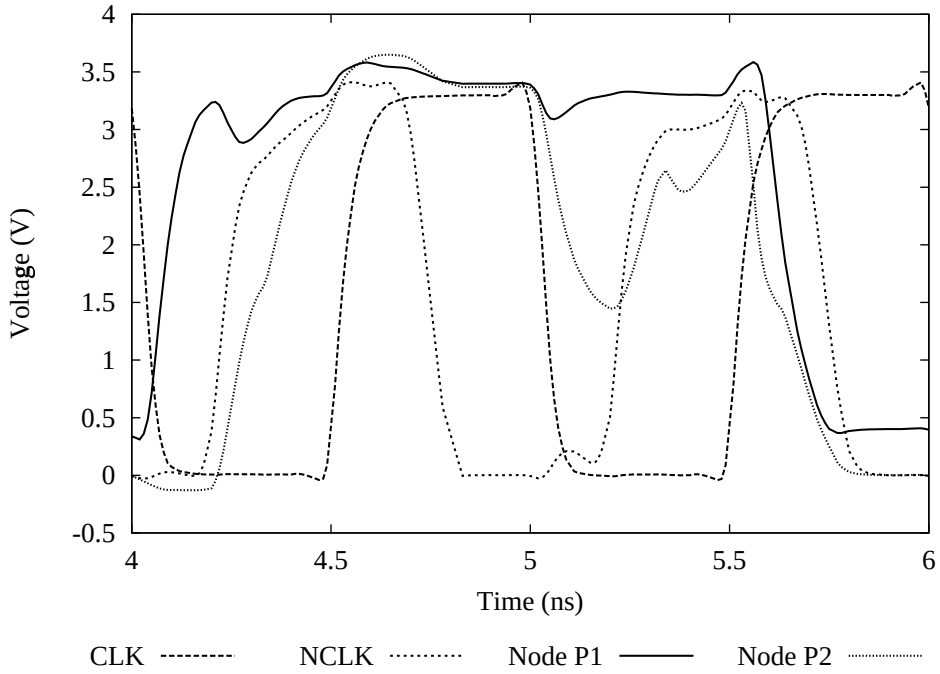


Figure 4.9: A transient analysis of a 2-input AND gate implemented with the proposed technique. The dynamic precharge P_1 node and P_2 node suffer charge redistribution problems.

dc path from P_2 to ground is formed through M_P and the NMOS transistor of the last inverter in the delay circuitry. If in the previous evaluation phase P_2 remained high, now it will suffer a logic level degradation (see Fig. 4.9 at approximately 5.2 ns). When NCLK rises again, a direct path to voltage supply is formed through the PMOS transistor of the last inverter in the delay circuitry and M_P. P_2 recovers its HIGH logic level.

Although these charge redistribution problems do not affect the functionality of the technique, they generate an additional power consumption in the circuit.

4.1.6 Application to a TSPC OR Gate

Other advantage of the proposed technique is that can be easily applied to different logic functions of the PDN block. The circuitry that gives the increased noise tolerance [delay, M_N and M_P in Fig. 4.2(a)] is not altered. For instance, a 4-input OR gate is formed by replacing the PDN of Fig. 4.7 (the two series transistors) by four parallel NMOS transistors, as shown in Fig. 4.10.

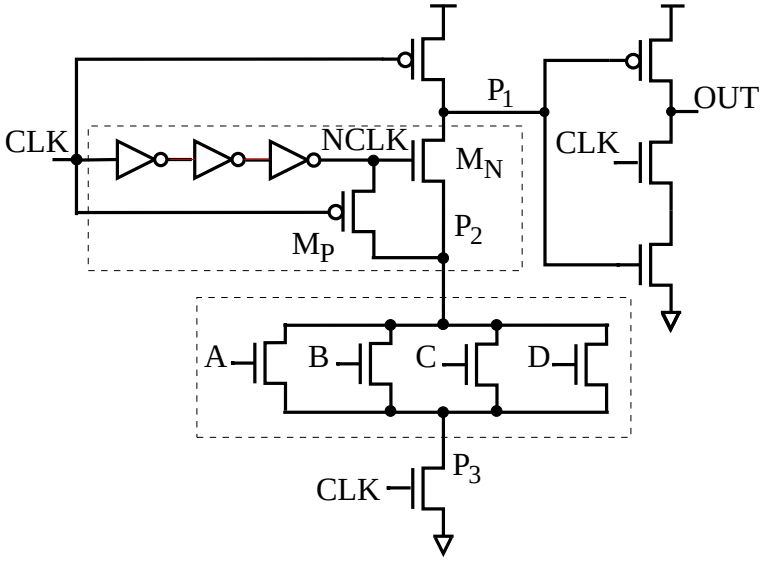


Figure 4.10: A 4-input OR gate with Proposed technique.

Fig. 4.11 shows an HSPICE simulation of the noise tolerant OR gate. The clock frequency and voltage supply were the same as in the case of the AND gate in the previous subsection.

For the case of OR gates, the first charge redistribution problem, described in subsection 4.1.5, becomes more significant. This is because the capacitance of the internal P_2 node is greater than that of the P_1 node for wide OR gates. So, the final voltage in the charge sharing process tends to be a small fraction of the voltage supply V_{dd}.

The final voltage in the charge sharing process can be approached by [71]:

$$V_f = \frac{1}{1 + \frac{C_{P2}}{C_{P1}}} \cdot V_{dd} \tag{4.3}$$

where C_{P1} and C_{P2} are the capacitances of the nodes P_1 and P_2, respectively. As C_{P2} becomes greater than C_{P1}, the final voltage V_f decreases. As a consequence, in wider OR gates the first charge redistribution problem above mentioned is more accentuated as it can be seen in Fig. 4.12 at approximately 4.2 ns. Finally, the second charge redistribution problem mentioned in subsection 4.1.5 affects in the same way to OR gates. With a careful device sizing it is possible to reduce these drawbacks.

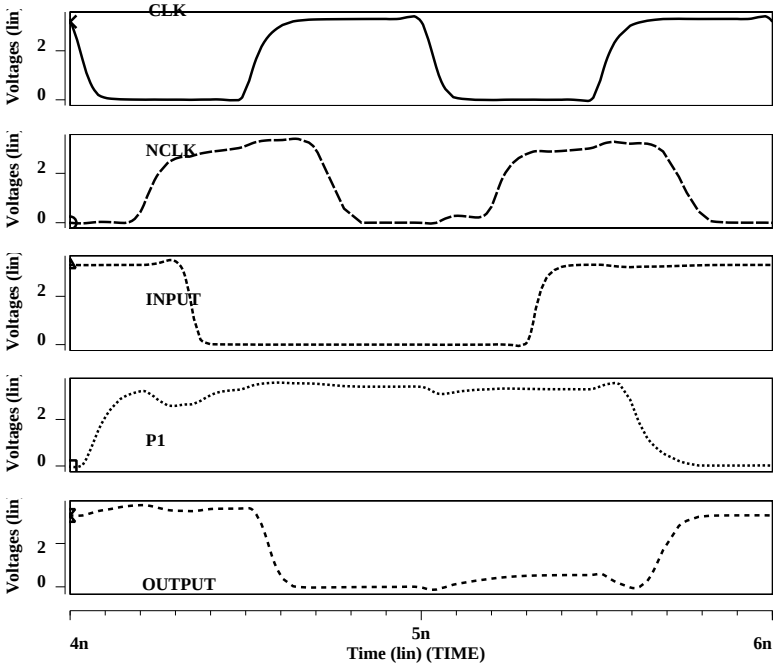


Figure 4.11: A transient analysis of a 4-input OR gate implemented with the proposed technique.

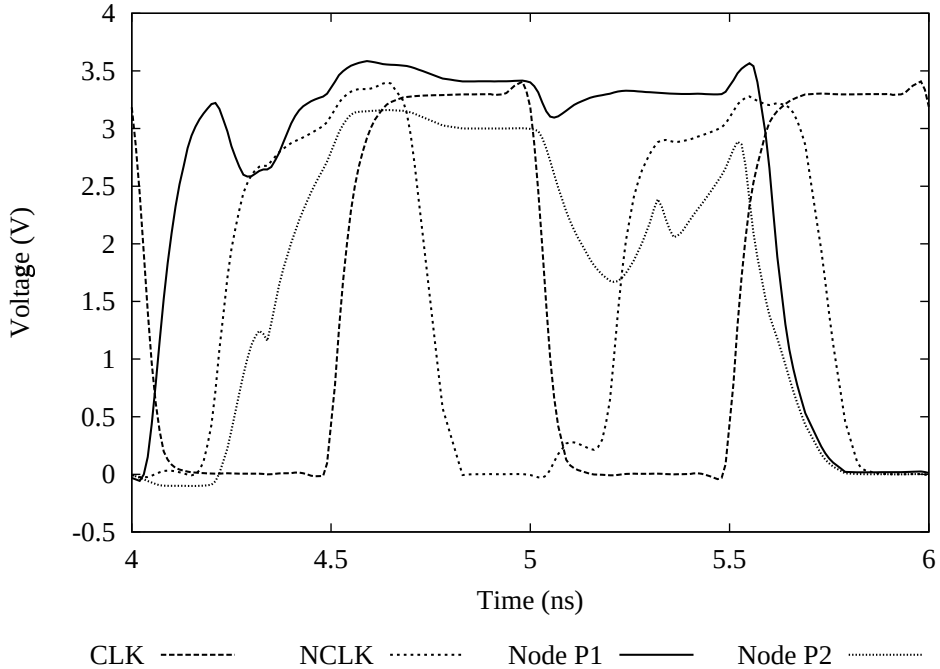


Figure 4.12: A transient analysis of a 4-input OR gate implemented with the proposed technique. The dynamic precharge P_1 node and P_2 node suffer charge redistribution problems.

4.2 Proposed Technique Performance

In this section the performance of the proposed technique is analyzed through HSPICE simulations. Noise tolerance, delay and power consumption are measured and a wide variety of dynamic gates are considered.

4.2.1 Transparency Window Characterization

In this subsection different gates implemented with the proposed technique have been considered. The purpose of this analysis is to explain the transparency window dependence on the fan-in, –and thus, on the discharge time of the dynamic precharge node (P_1)–, for a wide variety of logic gates. In order to have a qualitative estimation of this dependence a number of different gates were simulated using HSPICE and the parameters listed in Table 4.1.

Table 4.1: Simulation parameters.

Parameter	Description
Technology	0.35 μm AMS
Channel length	0.30 μm
Min. gate width	0.6 μm
V_{tp}	-0.62 V
V_{tn}	0.46 V
V_{DD}	3.3 V
MOSFET model	BSIM3v3
Data/Clock slopes of ideal signals	100 ps
Clock duty-cycle	50%
Delay calculation	Between 50% points
Clock frequency	1.5 GHz for latches and 1 GHz for gates

In Fig. 4.13 the different gates that were used in the simulations are shown. The circuitry enclosed by the dotted square determines the type of gate and the number besides the transistors indicate the corresponding transistor width. As noted, all gates have same transistor sizes. 4-, 6-, 8- and 12-input OR gates were simulated, as well as 2- and 4-input AND gates and a complex 16-input gate whose PDN has 4 branches with 4 series transistor in each branch. The delay circuitry was sized to generate a NCLK signal which permit a correct gate operation.

Fig. 4.14 and Fig. 4.15 show the ranges of the transparency window width for the OR and AND gates with a fan-out of four and twenty identical TSPC P-latches, respectively. The

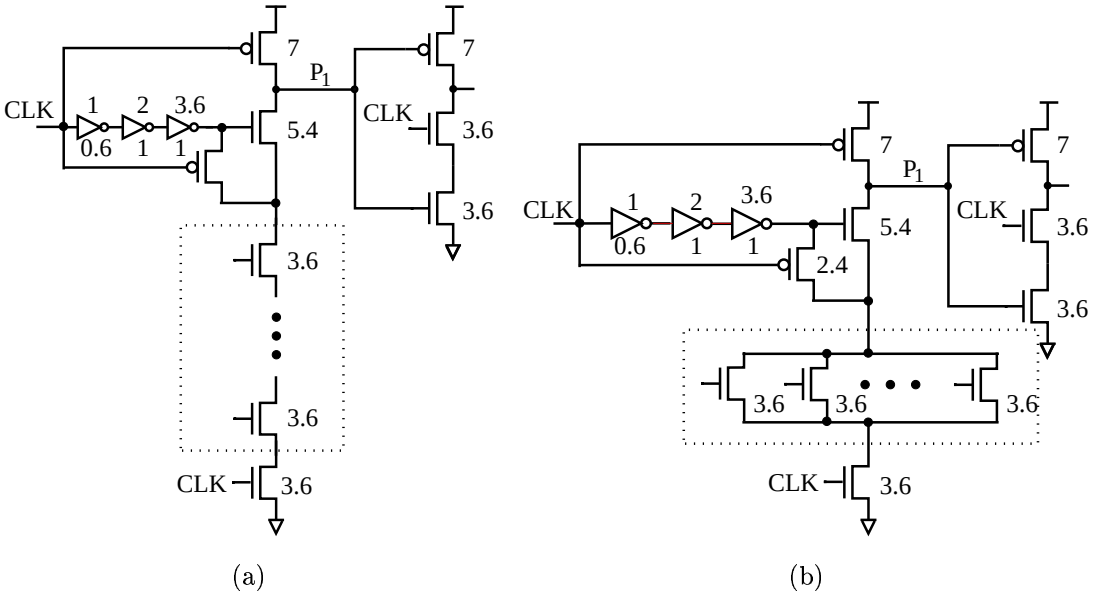


Figure 4.13: General inputs AND- (a) and OR-type (b) TSPC gates with the proposed technique.

symbol "■" marks the point of the minimum transparency window width for a safe operation. Below that point, the gates would have logic failure. Above that point, logic functionality is asserted at the cost of fewer noise tolerance.

As Fig. 4.14 and Fig. 4.15 show, the minimum transparency window width is almost the same for the simulated OR gates and varies approximately from 143 ps to 163 ps. This corresponds to a variation of scarcely 14%. On the other side, the minimum transparency window width is strongly dependent on the number of series transistors in the PDN (fan-in). In a 2-input AND gate four transistors are stacked in the pull-down path and in a 4-input AND gate, six transistors are needed. Accordingly, the discharge path is increased and more internal nodes need to be discharged. This slow down the propagation delay of the gate and, consequently, increase the need for a wider transparency window. As an example, the 2-input AND gate needs a minimum transparency window of about 155 ps and the 4-input AND gate needs one of about 233 ps, this corresponds to an increase of 50%, which is bigger than that for the OR gates. So, it is expected that the window size will be less dependent on the fan-in for OR gates.

The transparency window width does not need to be resized when the fan-out of the gate

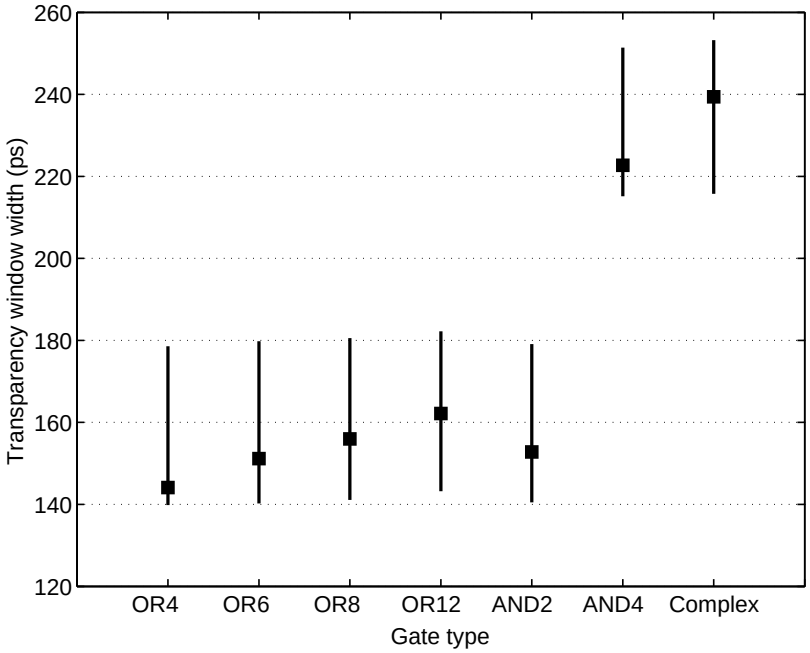


Figure 4.14: Ranges of the transparency window for different gates with a fan-out of 4 identical TSPC P-latches.

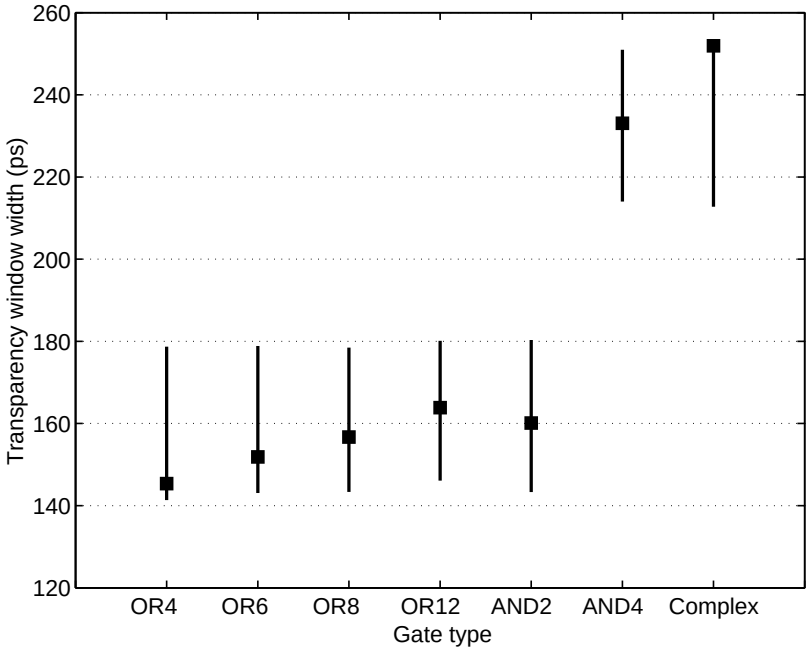


Figure 4.15: Ranges of the transparency window for different gates with a fan-out of 20 identical TSPC P-latches.

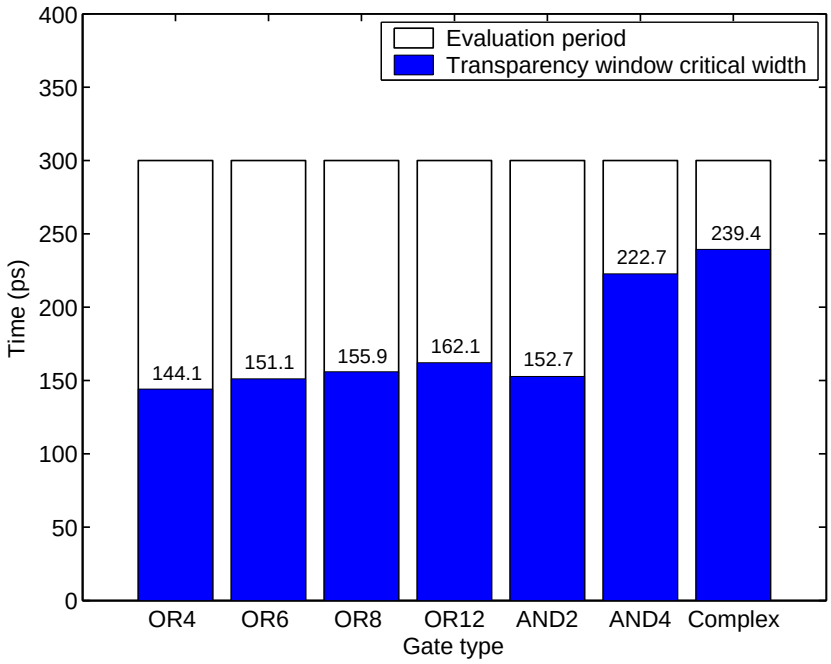


Figure 4.16: Transparency window critical width for gates with a fan-out of 4 identical TSPC P-latches.

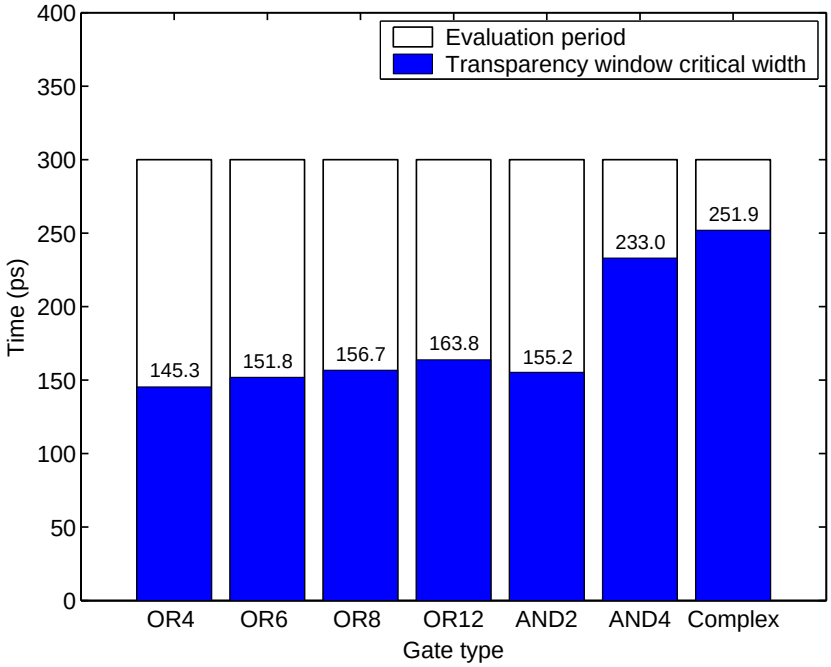


Figure 4.17: Transparency window critical width for gates with a fan-out of 20 identical TSPC P-latches.

is increased in wide OR gates and only a slight increase is needed in AND gates, see Fig. 4.14 and Fig. 4.15. The little dependence on the fan-in for OR gates is because parallel transistors have less delay penalty than series transistors in a PDN. Obviously, the wider fan-in the bigger the critical transparency window. Nevertheless, this increment is still smaller than that for AND gates.

The transparency window critical width is plotted together with the evaluation period in Fig. 4.16 and Fig. 4.17 for fan-outs of 4 and 20, respectively. In Table 4.2 the transparency window critical widths are listed. δ_{FI} and δ_{FO} indicate the necessary transparency window width increment with respect to the smaller fan-in and fan-out, respectively, when fan-in and fan-out change, respectively. For OR gates there is no need to resize the transparency window when fan-in is increased. However, for AND gates the more the fan-in the wider the transparency window size. For instance, the transparency window has to be increased by δ_{FI}=45.8% and δ_{FI}=50.1% when an 2-input AND gate becomes a 4-input AND gate for fan-outs of 4 and 20, respectively. (see Table 4.2). On the contrary, when a 4-input OR gate becomes a 12-input OR gate only an average increase of δ_{FI}=12.6% is needed (see Table 4.2). Finally, when the fan-out is increased there is practically no need to resize the transparency window as the maximum δ_{FO}, which corresponds to the 4-input AND gate, is 4.6%. The average transparency window increment is δ_{FO}=2%.

Table 4.2: Transparency window critical widths (ps).

FAN-OUT	AND2	AND4	δ_{FI} (%)	OR4	OR6	OR8	OR12	δ_{FI} (%)	Complex
4	152.7	222.7	45.8	144.1	151.1	155.9	162.1	12.5	239.4
20	155.2	233.0	50.1	145.3	151.8	156.7	163.8	12.7	251.9
δ_{FO} (%)	1.6	4.6		0.8	0.5	0.5	1.0		5.2

4.2.2 Optimization of the Proposed Technique

The performance-noise immunity trade-off of the proposed technique is brought to the forefront when the size of the precharge transistor M_P is changed [see Fig. 4.2(a)]. If W_{M_P} is increased, the precharge of the internal node is faster and a full V_{DD} level can be reached before the beginning of the evaluation phase for a predetermined clock frequency. Thus, better noise immunity due to the body effect is obtained (see section 4.1), as can be seen in Fig. 4.18.

However, the delay also increases due to the added parasitic capacitance in the internal precharge node. In Table 4.3 it can be seen that the wider the precharge transistor the longer cell delay is reached.

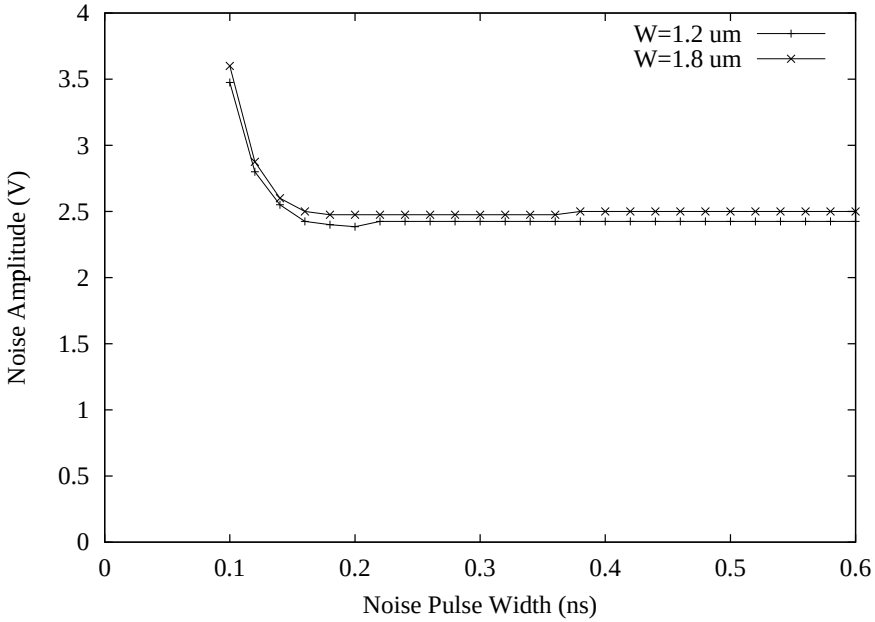


Figure 4.18: Noise tolerance dependence of the proposed technique on precharge transistor width W_{M_P} for a 2-input AND gate.

Table 4.3: Delay dependence of an AND gate with the proposed technique on M_P size.

W_{M_P} (μm)	Delay (ps)
0.6	224.2
0.9	226.3
1.2	229.1

Other important issue in the optimization process of the proposed technique is the selection of the precharge node in the PDN of the gate. Let's analyze the 2-input AND gate, see Fig. 4.7. Several simulations were done changing the precharge node from P_2 to P_4 to obtain different noise tolerances and delays for this gate. The best noise immunity is achieved when the node P_3 is precharged, and precharging the node P_2 the second noise immunity is obtained, see Fig. 4.19. The best delay case is obtained when the node P_2 is precharged and the best $ANTE$/Delay ratio is reached when the node P_3 is precharged, see Table 4.4. So, node P_2 is

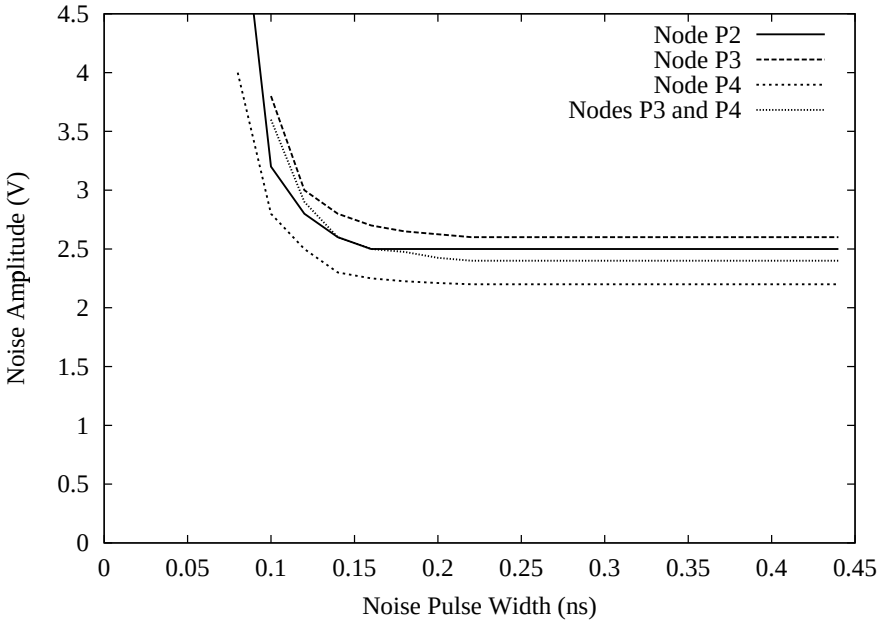


Figure 4.19: Noise tolerance dependence of the proposed technique on the precharged node for a 2-input AND gate.

selected to be precharged because the PDN is not altered and there is flexibility to incorporate logic into the gates.

For wide OR gates, see Fig. 4.10, there is no need to make this analysis because it is obvious that the best noise tolerance case is reached when the node P_2 is precharged.

Table 4.4: Delay dependence of an AND gate with the proposed technique on the precharged node, ($W_{M_P} = 0.6\mu m$).

Node	Delay (ps)	ANTE ($V^2 - ps$)	$\frac{ANTE}{Delay}$ (V^2)
P_2	224.2	1726.34	7.7
P_3	231.5	1898.30	8.2
P_4	227.3	1341.07	5.9
P_3 and P_4	242.6	1625.42	6.7

4.2.3 Comparison with other Techniques

In order to validate the proposed noise tolerant technique it is necessary to compare its behavior with that of previous techniques. The design parameters that we take into account to make the

comparison are:

- **Noise tolerance.** Noise immunity curve, Average Noise Threshold Energy (ANTE) and ANTE/delay are determined for the noise tolerant techniques.
- **Power consumption.** The average power consumption is measured for the whole circuit.
- **Delay.** The delay is measured at 50% points from the rising clock edge to the output.

Simulation results for AND gates

Twin-transistor, and Bobba's technique are chosen for comparison purposes. The conventional TSPC 2-input AND gate is also considered in order to have an initial reference, i. e. to measure the increase in noise tolerance. Fig. 4.20 shows the 2-input AND gates used in the simulations, the number besides the transistors indicate the transistor width. Although Twin-transistor and Bobba's techniques were proposed for Domino circuits, they are used in TSPC circuits only for comparison purposes.

To extract the parameters of interest, a test bench is set up to provide realistic simulation, see Fig. 4.21. In the simulation specifications the inputs can be tied to a buffer (normal operation) or to a noise signal (operation under noise), as represented by the switch in Fig. 4.21. In operation under noise, the noise pulse injected at one or all of the gate inputs is characterized by its width (W_n) and its amplitude (A_n). The rest of the inputs and the clock are driven by static inverters to provide realistic simulation, see Fig. 4.21. During the simulation under noise the noise pulse injected at one input, if it has sufficient width and amplitude, i. e., energy, is propagated through the output of the N-latch. Therefore, the state of the P-latch switches and, when this occur, the corresponding noise width (W_n) and amplitude (A_n) are registered to build the noise immunity curve (NIC).

First, the CLK-output delay for the AND gates under analysis is measured in absence of noise, see Fig. 4.22. Bobba's technique has the highest delay penalty followed by the here proposed technique. Twin-transistor technique has the smallest delay penalty, however, its noise immunity improvement is smaller than in the other techniques. It is important to mention that all noise tolerant techniques worked properly for 2-input AND gates at the specified clock frequency. This is not the case for wide OR gates, as it can be seen below.

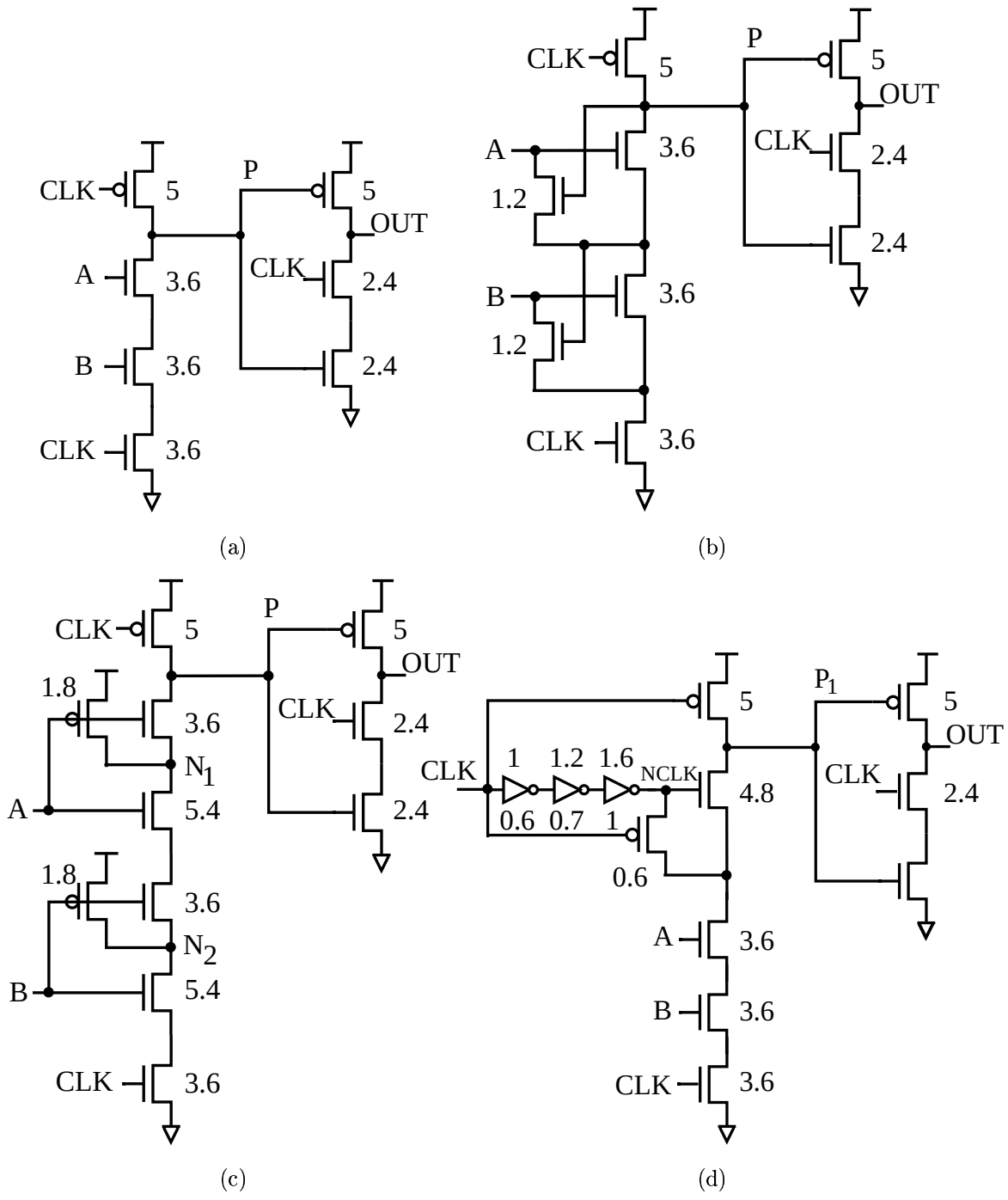


Figure 4.20: 2-input TSPC AND gates: (a) Conventional TSPC, (b) implemented with Twin-transistor technique, (c) with Bobba's technique, and (d) with the proposed technique.

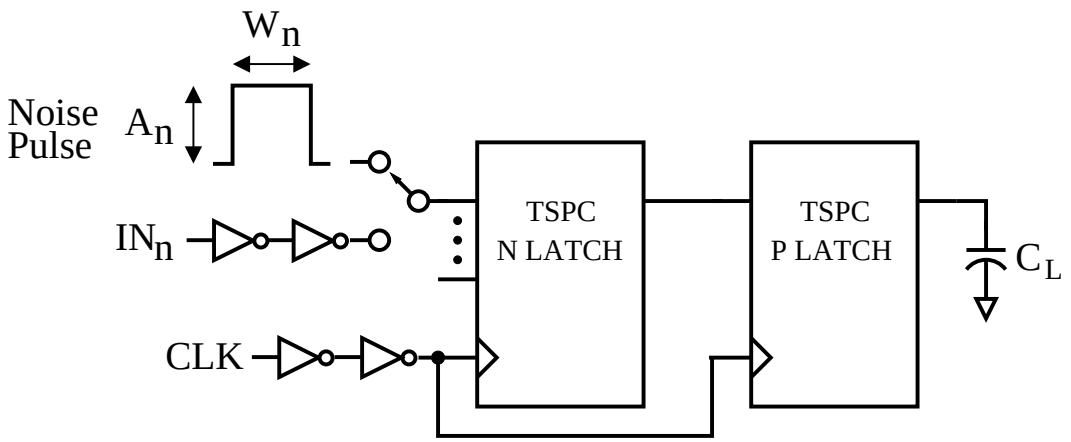


Figure 4.21: The simulation test bench.

Fig. 4.23 shows the noise immunity curve for 2-input AND gates implemented with Twin-transistor, Bobba's and proposed technique as well as a 2-input conventional logic gate. As it can be seen, the proposed technique has better noise immunity than the existing ones. In Table 4.5 we can observe that the proposed technique has the highest Average Noise Threshold Energy *ANTE* metric [60].

Moreover, delay measures indicate a delay penalty of 21.5% in proposed technique against 73.8% in Bobba's technique and 10.5% for Twin-Transistor technique for AND gates (see Table 4.5).

Table 4.5: Performance for 2-input TSPC AND gate.

TECHNIQUE	Power (mW)	$ANTE$ (V^2ps)	Delay (ps)	$\frac{ANTE}{Delay}$ (V^2)
Conv. dynamic	1.32	656	184.4	3.55
Twin-transistor	1.40	1003	203.8	4.92
Bobba's	1.63	1858	320.6	5.79
This work	1.70	2227	224.2	9.93

All the noise tolerant techniques increase the *ANTE* at the expense of an increased delay, power consumption or area. This is the case for our proposed technique. So, the main aim of the noise tolerant techniques is to increase the noise tolerance of a circuit with the less performance degradation. The ratio between *ANTE* and delay in Table 4.5 indicates how techniques are efficient to increase the noise immunity with a slight delay penalty. The proposed technique has

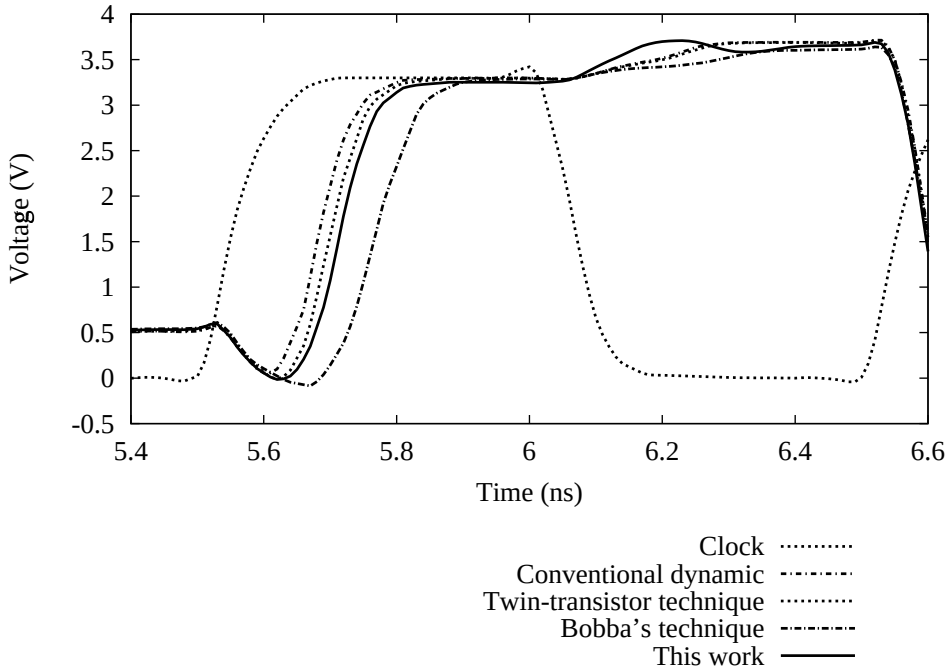


Figure 4.22: Output delay of the conventional TSPC 2-input AND gate and noise immune TSPC 4-input AND gates.

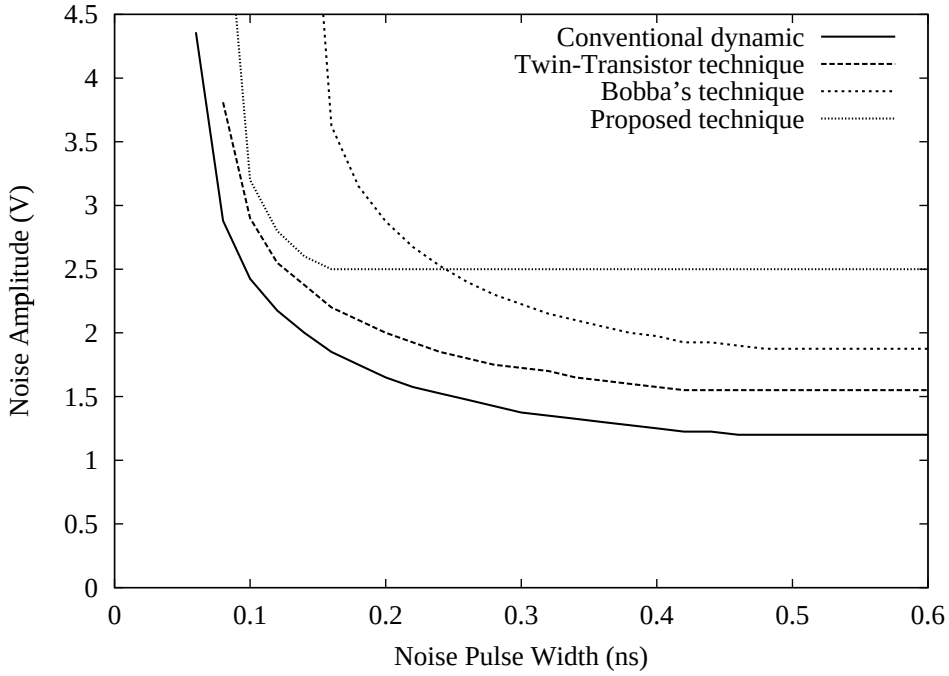


Figure 4.23: Noise immunity curves of AND gates.

the highest *ANTE*-Delay ratio for AND gates. Other important characteristic of the proposed technique is that for wide noise pulses the tolerated noise amplitude is higher than for the other techniques, see Fig. 4.23. This fact can be further exploited in future technologies because the peak noise value scales and noise pulse width increases with voltage scaling [62].

Simulation results for OR gates

Wide-OR gates have the advantage that components like decoders and comparators can be implemented in a single logic gate. Thus, it is of interest to analyze the performance of wide-OR gates implemented with the proposed technique. OR gates simulations were done using the same technology parameters of AND gates listed in Table 4.1. Fig. 4.24 shows the schematic diagram of conventional TSPC OR gate and TSPC OR gates implemented with the noise tolerant techniques. The numbers beside the transistors indicate the transistor width used in the simulations. As it can be seen, the different gates are equally sized in order to have a point of reference in the comparison.

To have a more realistic simulation the inputs and the clock were buffered. Two cases were considered. First, a pseudo-random data sequence was applied at one input while the remaining inputs were fixed to ground. Second, all inputs were excited by the pseudo-random data sequence. A pseudo-random data sequence is used to measure the average power when the data activity factor is α=0.5. We use two input conditions because some techniques present different performance for each one as can be seen below.

4-input OR gates are initially considered. Note that in the proposed technique the PDN is the same as the conventional logic. So, the fan-in can be easily changed by placing one transistor per additional input. However, Twin-transistor and Bobba's techniques, respectively, need two and three extra transistors per additional input. For example, in a 10-input Domino AND gate Twin-transistor and Bobba's techniques need 10 and 20 additional transistors, respectively. On the other side, the proposed technique always needs 7 additional transistors. So, for large fan-in gates is expected that the proposed technique has the lowest area penalty.

Fig. 4.25 shows the delay of the different 4-input OR gates when only one input goes high. As it can be seen, in this case Bobba's technique is even faster than conventional dynamic. First, when the input remains HIGH for more than one clock cycle, the precharge dynamic node

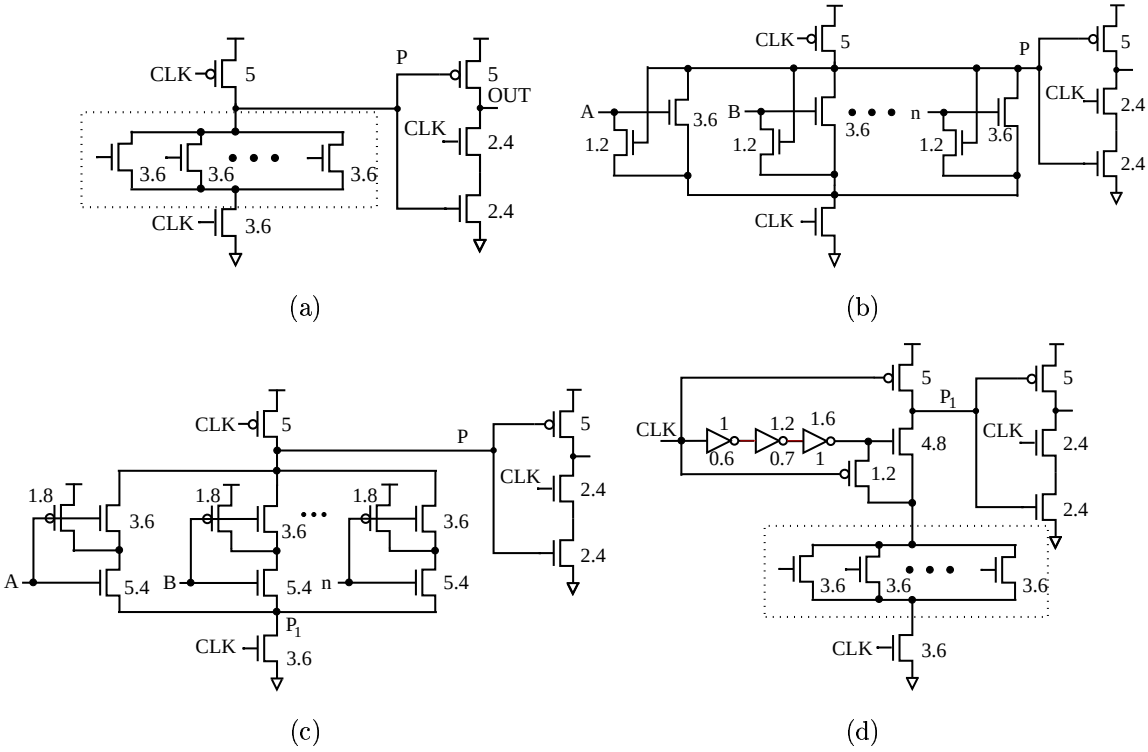


Figure 4.24: Wide-input TSPC OR gates: (a) Conventional TSPC, (b) implemented with Twin-transistor technique, (c) with Bobba's technique, and (d) with the proposed technique.

(P) cannot reach a complete HIGH logic level in precharge phase. This is due to a charge redistribution from P node to internal P_1 node [see Fig. 4.24(c)]. P_1 node has discharged in the previous clock cycle. This problem increases as the fan-in increases. Second, assuming the precharge P node has rose to V_{dd}, when the input rises to HIGH in precharge phase the charge redistribution occurs again. Hence, P node discharges before evaluation phase occurs and the output has an early logic transition. This is why this technique becomes faster than conventional dynamic logic.

Twin-transistor technique has static power consumption when at least one input remains LOW in precharge phase. As mentioned in 3.4.6 the inputs of a gate implemented with this technique require to be driven by static inverters. If during precharge phase (CLK="0") one input goes HIGH and the rest remain LOW the twin-transistors of the inputs act as pass transistors and a path between V_{dd} and GND is formed, causing a logic level degradation in the precharge P node. Fig. 4.26 shows the transient response of the 4-input Twin-transistor OR

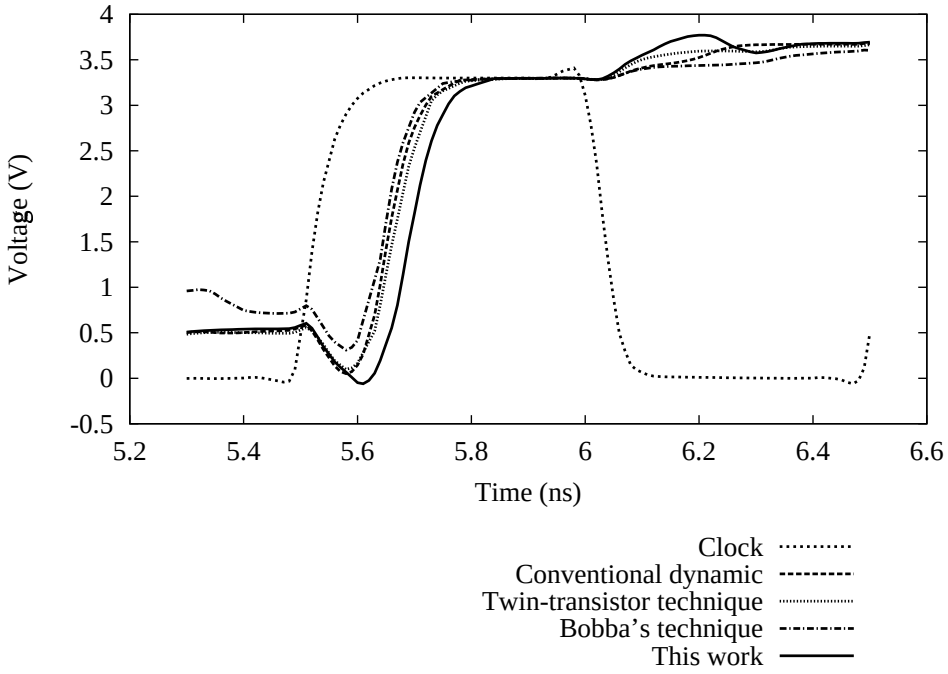


Figure 4.25: Output delay of the conventional TSPC 4-input OR gate and noise immune TSPC 4-input OR gates. Only one input goes high.

gate when only one input goes high. The arrows indicate the logic level degradation caused by the static power consumption conflict during precharge phase.

When all inputs rise in precharge phase the Twin-transistor technique has no more static power dissipation. Bobba's technique presents more inconveniences. Fig. 4.27 shows that when all inputs are HIGH in precharge phase the precharge node can not rise to V_{dd} or discharges prior to evaluation phase.

Table 4.6: Performance for 4-input TSPC OR gate when only one input goes high.

Technique	Power (mW)	$ANTE$ (V^2ps)	Delay (ps)	$\frac{ANTE}{Delay}$ (V^2)
Conv. dynamic	3.2	1134	130.38	8.7
Twin-Trans. Tech.	4.2	1387	134.33	10.3
Bobba's Tech.	4.4	1788	121.48	14.7
Proposed Tech.	3.8	1830	168.9	10.8

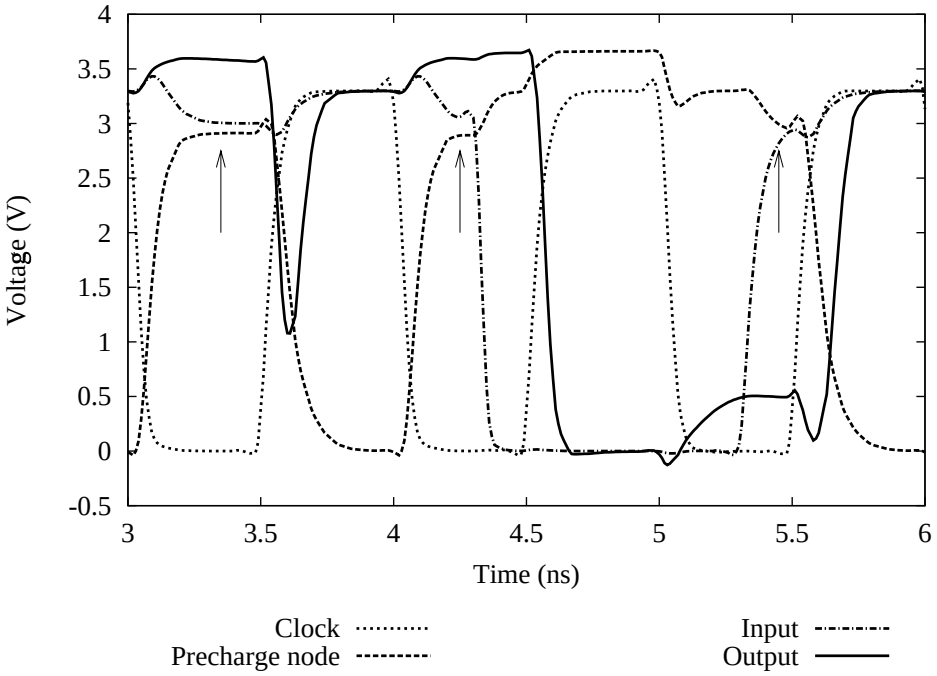


Figure 4.26: Transient response of the 4-input Twin-transistor OR gate when only one input goes high. Arrows indicate the cases where static power consumption occurs causing a logic level degradation in precharge node.

Table 4.6 and Table 4.7 resume the performance of the 4-input OR gates. Besides the increased power consumption and delay, the proposed technique improves the noise tolerance ($ANTE$) by 61% with respect to the conventional dynamic logic. The average power consumption penalty is 17.7% and can be reduced by sizing and sharing the delay circuitry between logic gates. The average delay penalty is 15.6%.

Twin-transistor and Bobba's techniques require more power consumption than the proposed technique for the case of 4-input OR gates. This is due the static power consumption and the added circuitry in both techniques. Furthermore, those techniques have less noise tolerance than the proposed technique. In this way, the performance degradation of the proposed technique can be supported by a rise in the noise tolerance.

Fig. 4.28 shows the noise immunity curves of 4-input OR gates. As previously stated,

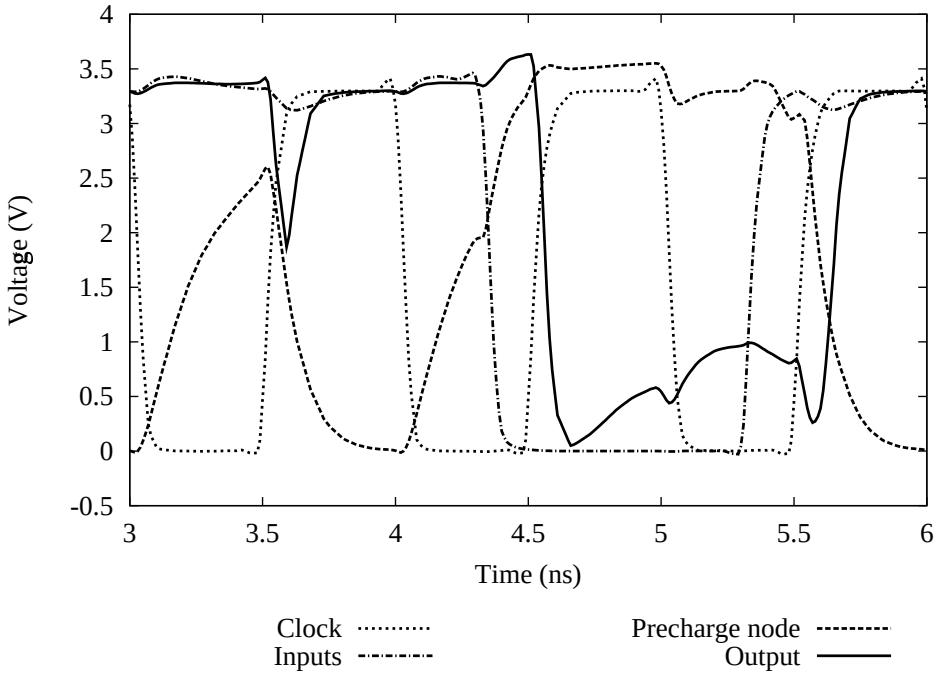


Figure 4.27: Transient response of the 4-input OR gate with Bobba's technique when all inputs go high. Precharge node cannot rise to V_{DD} due to the charge sharing problem.

the proposed technique has higher noise tolerance than the previous proposed techniques and the conventional dynamic gate.

Simulation results for 6-input OR gates show that in the Twin-transistor technique the power consumption when one input rises HIGH decreases as the fan-in increases. The reason is simple. For wider-OR gates more twin-transistors are trying to pull-down the precharge node through the transistor driven by the HIGH level input. So, the precharge node cannot be charged to a full HIGH logic level (see Fig. 4.30). This fact reduces the voltage swing of the precharge node and consequently the associated power consumption and the delay. However, as is illustrated in Fig. 4.30, when an input arrives late the precharge node voltage cannot be recovered and a logic failure occurs.

In Bobba's and proposed techniques there are no functional problems when only one input rises. Table 4.8 list the performance of 6-input OR gates when only one input rises. The proposed technique increases the noise tolerance of the conventional dynamic logic in 82.4%.

Table 4.7: Performance for 4-input TSPC OR gate when all inputs go high.

Technique	Power (mW)	$ANTE$ (V^2ps)	Delay (ps)	$\frac{ANTE}{Delay}$ (V^2)
Conv. dynamic	3.6	1134	212.33	5.34
Twin-Trans. Tech.	4.0	1387	216.43	6.40
Bobba's Tech.	5.1	1788	120.62	14.82
Proposed Tech.	4.2	1830	215.90	8.47

The power consumption and delay penalties are 16.9% and 17.7%, respectively.

Although Twin-transistor technique has the highest ANTE-delay ratio it is not the best option because the logic could fail. Consequently, the proposed technique is the best choice. When all inputs rise in the 6-input OR gates Bobba's technique gives the same kind of drawback than for the case of 4-input gates, i.e., the precharge node has no full swing. This can be severe if the fan-in increases. Fig. 4.31 shows that when inputs are HIGH the precharge node does not have a rail to rail swing.

Table 4.8: Performance for 6-input TSPC OR gate when only one input goes high.

TECHNIQUE	Power (mW)	$ANTE$ (V^2ps)	Delay (ps)	$\frac{ANTE}{Delay}$ (V^2)
Conv. dynamic	3.31	1288	145.87	8.82
Twin-transistor	3.74	1518	60.62	25
Bobba's	4.56	1938	196.63	9.85
Proposed Tech.	3.87	2350	171.8	13.67

Table 4.9: Performance for 6-input TSPC OR gate when all inputs go high.

TECHNIQUE	Power (mW)	$ANTE$ (V^2ps)	Delay (ps)	$\frac{ANTE}{Delay}$ (V^2)
Conv. dynamic	3.99	1288	142.11	9
Twin-transistor	4.13	1518	158.4	9.6
Bobba's	6.11	1938	189.85	10.2
Proposed Tech.	4.56	2350	171.17	13.7

Again, Twin-transistor technique has no problems when all inputs rise. So, we can compare the ANTE-delay ratio of the techniques. As Table 4.9 illustrate, the proposed technique has the highest ANTE-delay ratio. In this way, the proposed technique is effective in increasing the noise tolerance with a slight delay penalty. Bobba's technique becomes less energy-efficient as fan-in increases, so, it is not the choice for wide-OR TSPC noise tolerant circuits.

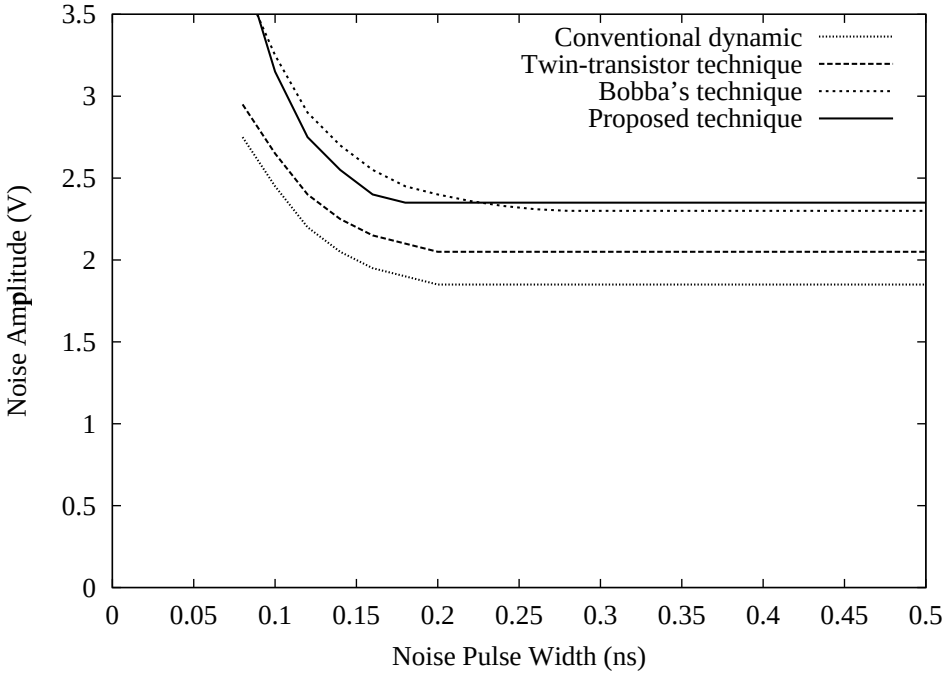


Figure 4.28: Noise immunity curves of 4-input OR gates.

In Fig. 4.32 the noise immunity curves for 6-input OR gates are shown. The proposed technique has better noise tolerance for any combination of noise pulse width and amplitude.

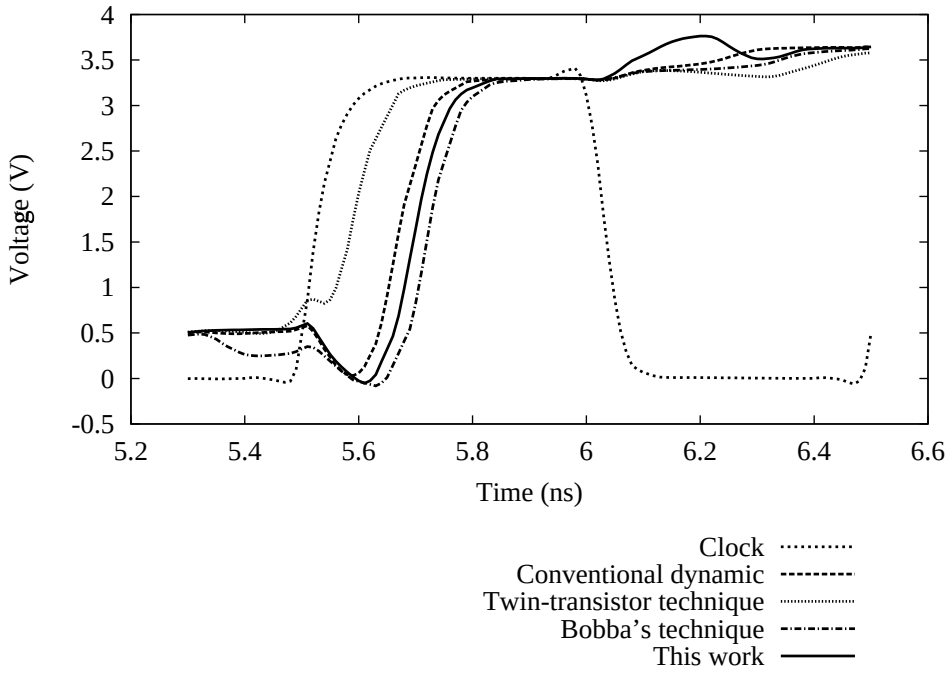


Figure 4.29: Output delay of the conventional TSPC 6-input OR gate and noise immune TSPC 6-input OR gates. Only one input goes high.

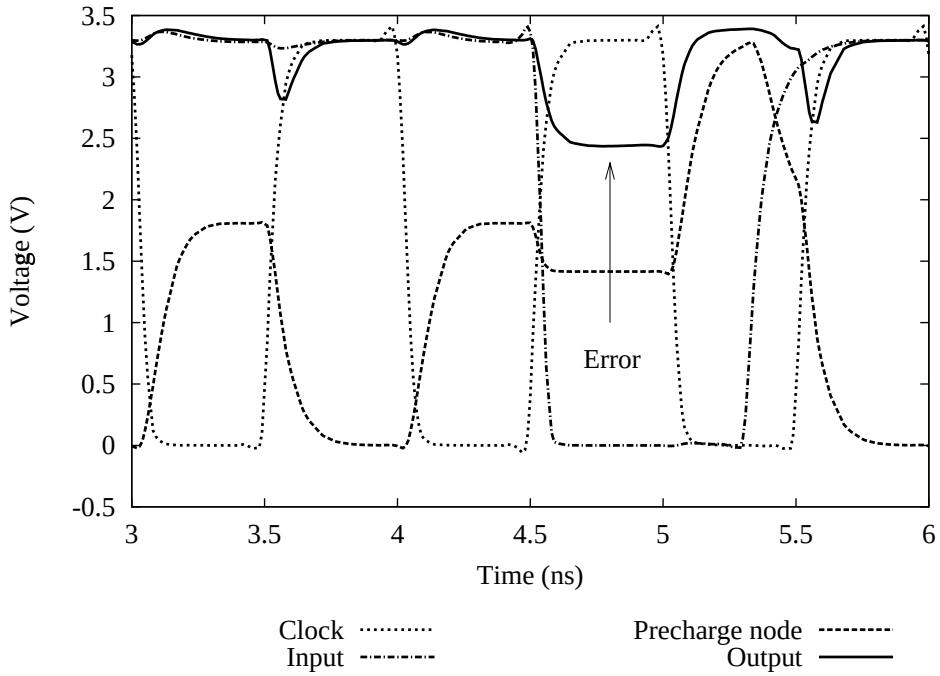


Figure 4.30: Transient response of the 6-input Twin-transistor OR gate when only one input goes high. Twin-transistor technique suffers static power consumption in a TSPC wide-OR gate when some inputs remain low. The logic level of the precharge node is degraded as arrows point.

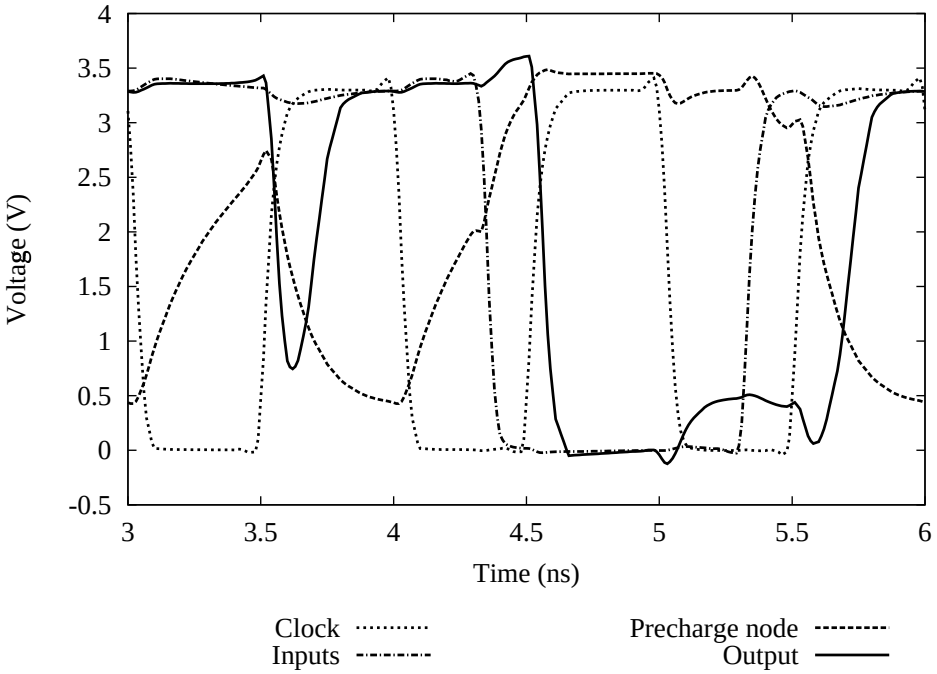


Figure 4.31: Transient response of the 6-input OR gate with Bobba's technique when all inputs go high. The parasitic capacitances in the PDN slow down the circuit and charge redistribution affects the zero logic level in precharge phase.

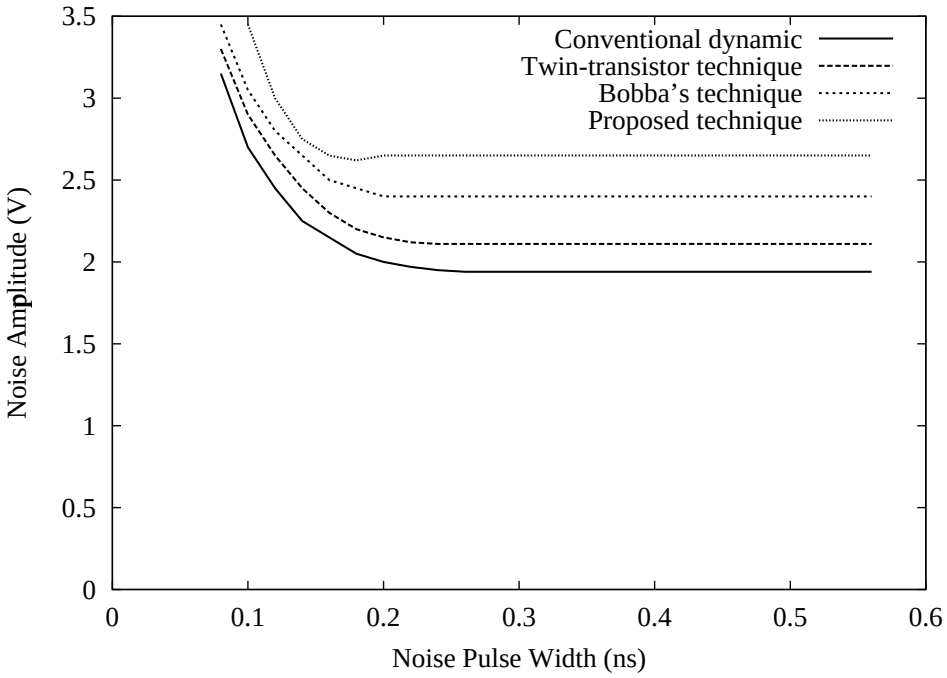


Figure 4.32: Noise immunity curves of 6-input OR gates.

4.3 Application to a Full Adder

To verify the noise immunity of the proposed technique in a relatively complex system we compare two fully pipelined 4-bit carry look-ahead full-adders. Full adders are implemented with conventional logic and with the proposed technique. The full adders are based on the logic diagram presented in [72], see Fig. 4.33. All the logic is incorporated in the N-blocks and P-blocks act only as delay elements. We use a TSPC latch as a load at every output of full adder. In the simulations, the power supply was $V_{dd} = 3.3V$ and the clock frequency was $f_{CLK} = 800MHz$.

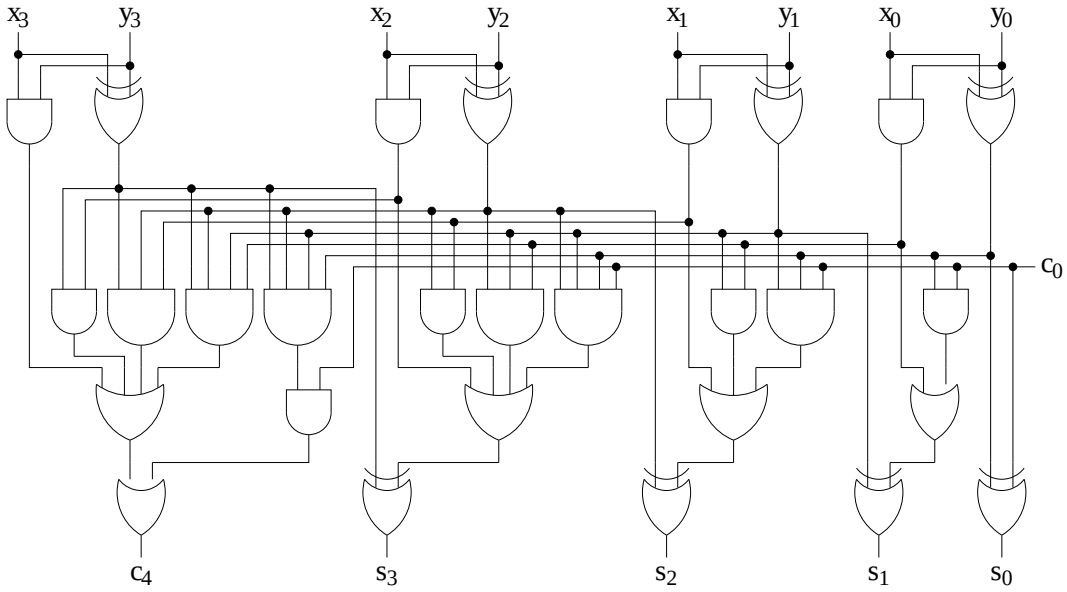


Figure 4.33: Logic diagram of the 4-bit carry look-ahead full adder.

The crosstalk noise was modelled by squared pulses in order to determine the noise amplitude and noise width in a direct way. These noise pulses were applied in several nodes at the inputs of N-blocks. Different noise immunity curves (NICs) were obtained and their average represented in a unique noise immunity curve.

The noise immunity curves (See Fig. 4.34) show that the 4-bit carry look-ahead full adder implemented with the proposed technique has better noise immunity than the conventional one. This is evident because the NIC of the noise immune full adder is completely over the NIC of the conventional one. The $ANTE$ of the conventional full-adder is $ANTE_c = 1300$ (V^2ps) and the $ANTE$ of the full adder with the proposed technique is $ANTE_p = 2811$ (V^2ps). Hence, the

proposed technique improves the $ANTE$ by 2.1 times over the conventional dynamic full adder. From Table 4.10, where the performance of both full adders is summarized, it can be seen that the power consumption and delay are increased by 1.58 times and 1.3 times, respectively, in the full adder with the proposed technique. However, the ANTE-delay ratio is incremented by 1.66 times in the full adder with the proposed technique over the conventional one. Again, the proposed technique trades off performance by noise immunity but this trade-off is acceptable considering the high ANTE reached.

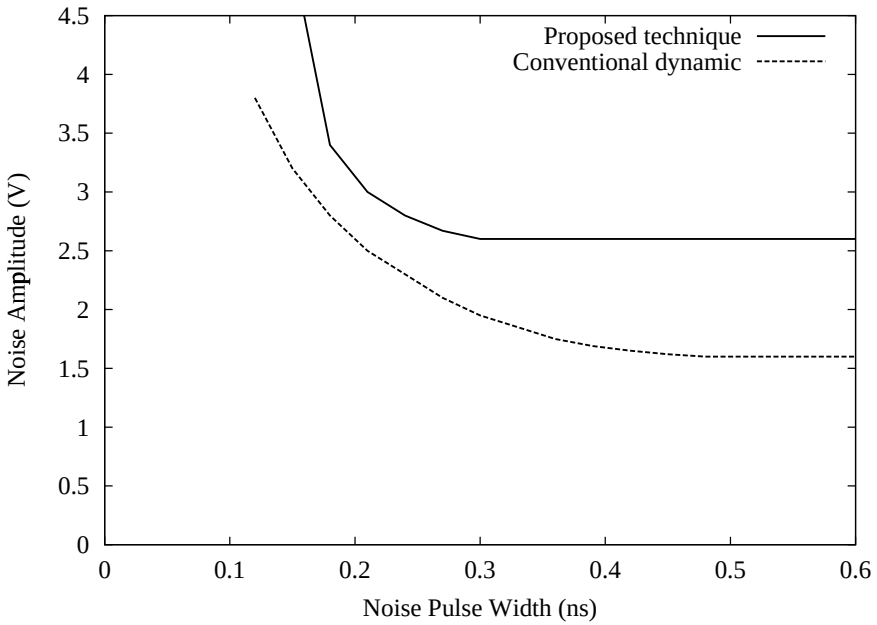


Figure 4.34: Noise immunity curves for full adders.

Table 4.10: Performance for 4-bit TSPC carry look-ahead full adders.

Technique	Power (mW)	$ANTE$ (V^2ps)	Delay (ps)	$\frac{ANTE}{Delay}$ (V^2)
Conv. dynamic	15.57	1300	180.52	7.2
Proposed Tech.	24.71	2811	235.12	11.95

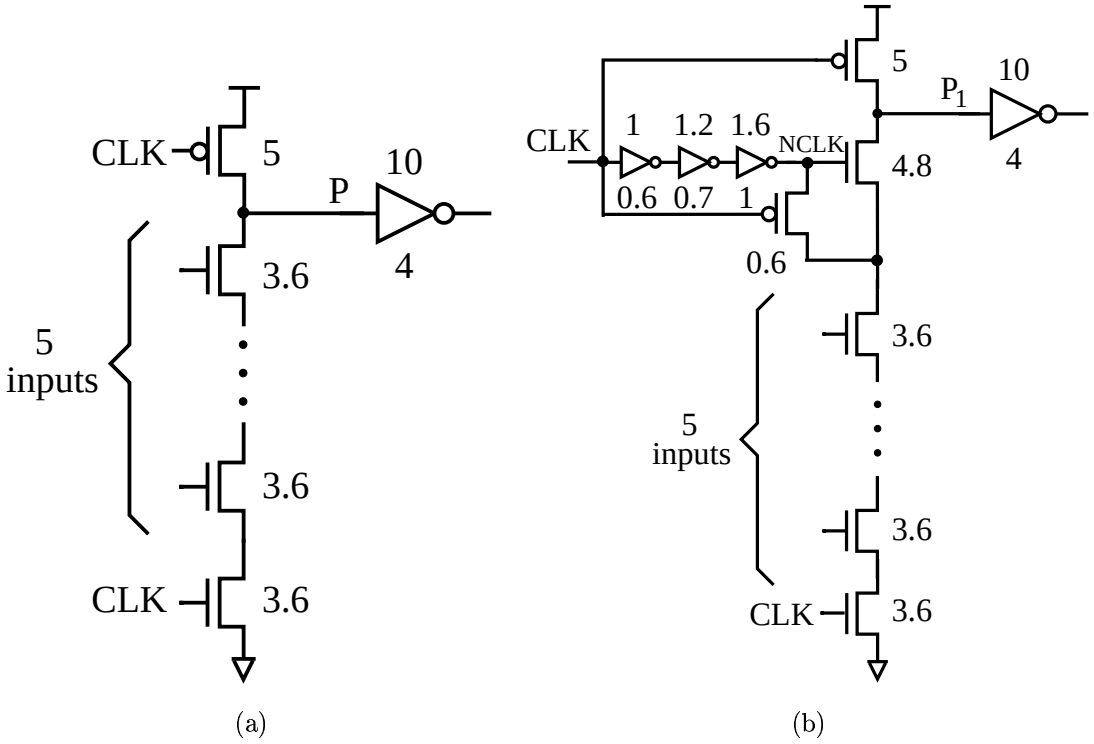


Figure 4.35: 5 input Domino AND gates: (a) Conventional, and (b) with the proposed technique.

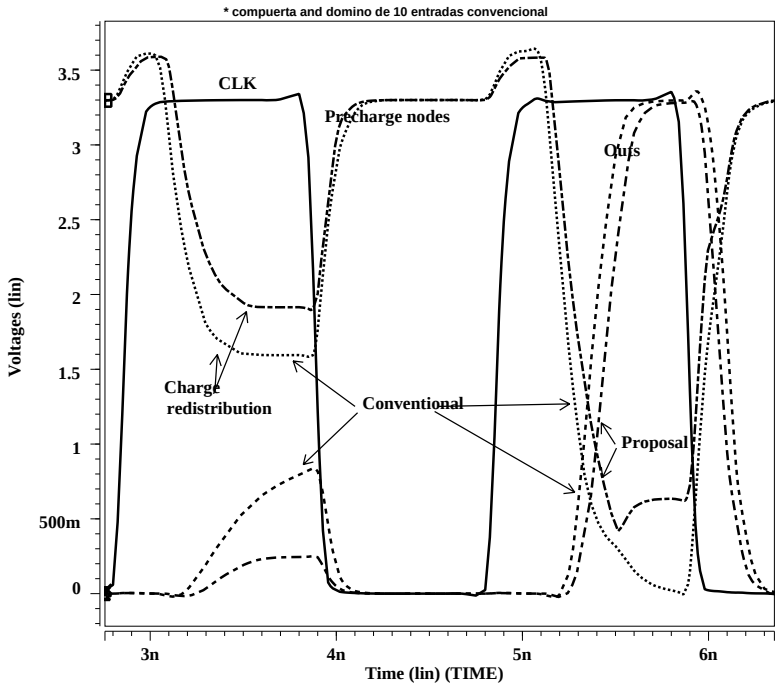


Figure 4.36: Time domain performance for a 5-input conventional Domino AND gate.

4.4 Extension to Domino Logic Style

The proposed noise tolerant dynamic circuit technique can be implemented in a variety of dynamic logic styles, this flexibility gives advantage over previous noise tolerant techniques. Next, the proposed technique is applied to a 5 input Domino AND gate (see Fig. 4.35). In this analysis the metric Unity Noise Gain (UNG) is employed.

Using the same simulation conditions as in previous analysis the two Domino AND gates were simulated at a clock frequency of f_{CLK}=500 MHz. One advantage of the proposed technique over the conventional Domino AND gate is that it reduces charge redistribution problems, see Fig. 4.36. Table 4.11 depicts the performance comparison of the conventional Domino AND gate and the one with the proposed noise tolerant technique. The power consumption increment is 1.2 times and the delay increment is 1.12 times in the noise immune gate. This performance degradation is a trade-off with the increased noise immunity, (see Table 4.11). The UNG is increased by 1.44 times in the gate implemented with the proposed technique over the conventional one and the UNG-delay ratio of the gate with the proposed technique is bigger than the conventional one by 1.28 times. Thus, the proposed noise tolerant technique also works properly for Domino gates.

Table 4.11: Performance for 5 input Domino AND gates.

Technique	Power (mW)	*UNG* (V)	Delay (ps)	$\frac{UNG}{delay}$ (V/ps)
Conv. dynamic	3.65	1.52	506.42	3.00
Proposed Tech.	4.41	2.20	568.88	3.86

4.5 Scaling Analysis of Noise Immunity in Dynamic Circuits

It has been explained that the noise tolerance of dynamic digital circuits is decreasing. Due to this fact, noise tolerant circuits are needed. In this section an analysis of the noise immunity scaling trends of the proposed technique applied to dynamic circuits is introduced. Conventional dynamic TSPC logic and Bobba's technique are also analyzed. First, a reliable scaling scheme is reviewed and a scalable SPICE transistor model is used in the analysis. Second, based in an

analytical model, the scaling trends of the noise immunity in a TSPC latch is presented. Finally, by means of simulations the scaling trends of dynamic circuits will be verified.

4.5.1 Scaling Strategy

In order to determine the scaling trends of the noise tolerance of dynamic digital circuits it is necessary to have an accurate scaling scheme. There are several scaling schemes that attempt to predict the transistor scaling, namely constant field scaling, quasi-constant voltage scaling and constant voltage scaling, among others. However, these scaling predictions have inaccuracies for submicron devices.

In [73] McFarland presents a scalable SPICE Level 3 device model. Using this model the noise immunity of any circuit can be simulated for a wide range of technologies. There are other models more accurate than the Level 3 model used in [73], but those models are based in a high number of empirical parameters which can not be scaled because they have no clear scaling trends. The Level 3 model is used in this work to determine the noise tolerance scaling trends in the dynamic digital circuits because has a reasonable trade-off of accuracy and complexity. Some of the device and model parameters as well as their scaling factors are rewritten in Table 4.12.

To verify that the scaling scheme proposed by McFarland predicts properly the industry trends we have plotted in Fig. 4.37 the supply and threshold voltage scaling trends given by the SIA Roadmap, by TSMC processes and by McFarland. As it can be seen the scalable Level 3 model (McFarland's model) predicts properly the V_{DD} and V_t scaling trends. Hence, the scalable Level 3 model is a good approximation to the real scaling. The V_{DD} and V_t projections are shown in Table 4.13.

4.5.2 Noise Immunity Scaling Trends: Analytical Results

To determine the noise immunity of dynamic CMOS circuits the analytical noise immunity model proposed in [74] was used. This model is based on the transistor engineering model presented in [75]. We consider the case where a positive noise pulse appears on a LOW input in a TSPC latch. To estimate the dynamic circuit noise tolerance, the circuit of Fig. 4.38(a) is used which can be the input stage of a TSPC or Domino latch. The second stage (a N-C^{2}MOS

Table 4.12: Transistor and model parameters scaling factors.

PARAMETER	SCALING FACTOR
$L_{drawn}\ (\mu m)$	$1/S$
$L_{eff}(\mu m)$	$1/S$
$XJ(nm)$	$1/S$
$V_{dd}(V)$	$1/S^{0.78}$
$TOX(NM)$	$1/S^{0.71}$
$NSUB(cm^{-3})$	$1/S^{1.27}$
V_t (V)	$1/S^{0.44}$
ΔV_{TD} (mV)	$1/S^{0.52}$

Table 4.13: V_{DD} and V_t scaling projection.

$L_{drawn}\ (\mu m)$	$V_{dd}\ (V)$	V_t (V)
0.45	4.2	0.88
0.35	3.5	0.79
0.25	2.7	0.68
0.15	1.8	0.54
0.05	0.7	0.33

or static inverter) has been omitted for simplicity and all the capacitances associated to node P have been lumped in capacitance C_L.

Suppose that the node P is precharged to V_{OH} and the clock (CLK) is high (evaluation phase). Then, a positive noise pulse appears on the input. The internal node of the NMOS chain is discharged because the bottom NMOS is on and transistor M_{N2} is working in linear operation region. Thus the NMOS chain can be simplified to one equivalent transistor (M_{eq}) working in saturation region if the noise pulse is higher than the threshold voltage V_t. Fig. 4.38(b) shows the equivalent transistor with the equivalent load capacitor at the output (C_L). The current through the load capacitor I_{C_L} is equal to the current through the equivalent transistor $I_{M_{eq}}$. M_{eq} enters the saturation operation region when the noise pulse amplitude goes above the equivalent transistor threshold voltage V_t. This can be expressed as follows:

$$I_{C_L} = I_{M_{eq}}$$

where

$$I_{C_L} = -C_L \frac{dV_P}{dt} \tag{4.4}$$

and $I_{M_{eq}}$ is the saturation current given by [75]. After replacing the drain current model for the

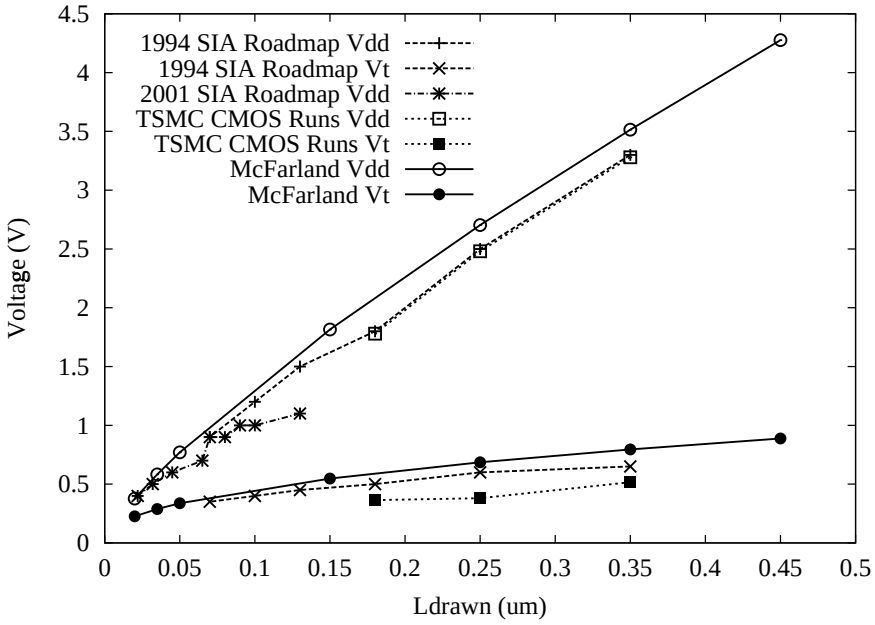


Figure 4.37: Several scaling scenarios for V_{DD} and V_t.

transistor M_{eq}, the following expression is obtained:

$$-C_L \frac{dV_P}{dt} = K\nu_{sat}C_{ox}W_{eff}(V_{GS} - V_T) \tag{4.5}$$

Rearranging the previous expression gives:

$$dt = -C_L \frac{dV_P}{K\nu_{sat}C_{ox}W_{eff}(V_{GS} - V_T)} \tag{4.6}$$

Integrating (4.6) through the time period where V_P discharges from V_{OH} to V_{IL}, gives:

$$\Delta t = \frac{C_L \left[1 + \frac{2\nu_{sat}L_{eff}(1+\theta(V_{GS}-V_T))}{\mu_0(V_{GS}-V_T)}\right](V_{OH} - V_{IL})}{\nu_{sat}C_{ox}W_{eff}(V_{GS} - V_T)} \tag{4.7}$$

The noise pulse amplitude applied to the latch input can be represented by A_n. Hence, V_{GS} can be substituted by A_n. At $V_{GS} = A_n$ the noise pulse width has to be at least $W_{n_{min}} = \Delta t$ for the output to reach V_{IL}. Substituting these parameters in equation (4.7) results in

$$W_{n_{min}} = \frac{C_L \left[1 + \frac{2\nu_{sat}L_{eff}(1+\theta(A_n-V_T))}{\mu_0(A_n-V_T)}\right](V_{OH} - V_{IL})}{\nu_{sat}C_{ox}W_{eff}(A_n - V_T)} \tag{4.8}$$

Figure 4.38: (a) Input stage of a conventional TSPC latch, (b) simplified model for the analysis.

Rearranging (4.8) for A_n an expression to estimate the necessary noise pulse amplitude to produce a logic transition on the output node is obtained:

$$A_n = V_T + \frac{K_1 + \sqrt{K_1^2 + 4W_{n_{min}} K_2 K_3}}{2W_{n_{min}} K_3} \tag{4.9}$$

where

$$K_1 = C_L \left(\mu_0 + 2\theta\nu_{sat} L_{eff}\right)\left(V_{OH} - V_{IL}\right)$$

$$K_2 = 2C_L \nu_{sat} L_{eff}\left(V_{OH} - V_{IL}\right)$$

$$K_3 = \nu_{sat} C_{ox} W_{eff} \mu_0$$

Some considerations should be taken into account for this model to represent more realistic circuits:

- Path equivalence, by taking the equivalent PDN width $W_{eq_{path}}$.
- The initial charge stored in the internal nodes.

Taking into account these considerations, the model in (4.9) is modified to:

$$A_n = V_T + (1 + K_n)\frac{K_1 + \sqrt{K_1^2 + \frac{4}{1+K_n} W_{n_{min}} K_2 K_3}}{2W_{n_{min}} K_3} \tag{4.10}$$

where

$$K_1 = C_L \left(\mu_0 + 2\theta\nu_{sat} L_{eff}\right)\left(V_{OH} - K_{1n} V_{IL}\right)$$

$$K_2 = 2C_L \nu_{sat} L_{eff} \left(V_{OH} - K_{1n} V_{IL}\right)$$

$$K_3 = \nu_{sat} C_{ox} W_{eq_{path}} \mu_0$$

$$K_{1n} = \frac{C_L + \sum_{i=1}^{n} C_i}{C_{out}}$$

$$K_n = \frac{Q_{en}}{Q_{en} + Q_t} \qquad where \qquad Q_{en} = \sum_{i=1}^{n} C_i V_i$$

Q_t is the initial charge stored on the output node and n is the number of internal nodes in the PDN.

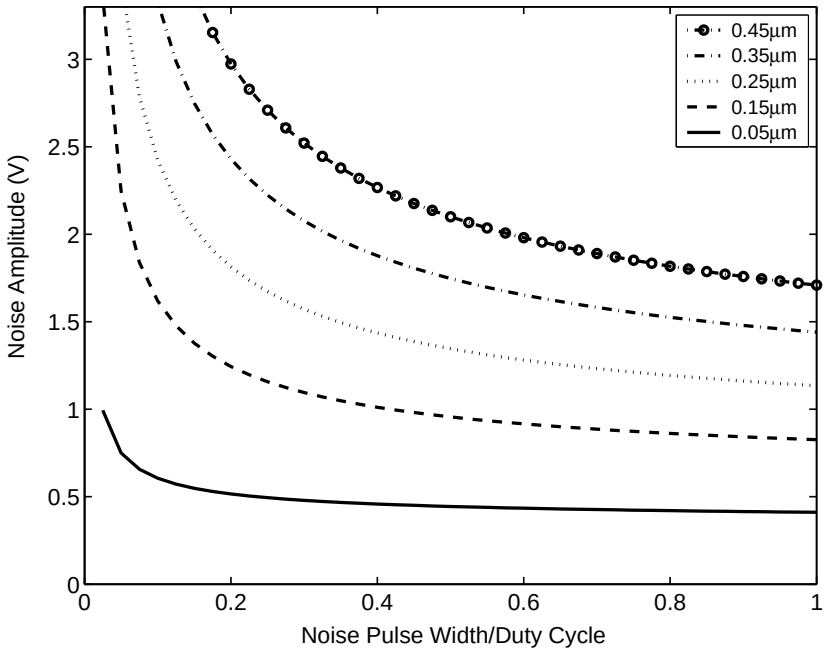


Figure 4.39: Noise immunity curves for the TSPC conventional latch using Kabbani's model.

As many references cite, the signal integrity problem in integrated circuits is becoming a main concern as technology scales. Using (4.10) and the scalable Level 3 model the noise immunity curves [50] for the conventional TSPC latch (modeled in Fig. 4.38) have been plotted in Fig. 4.39. To include all the noise immunity curves for different transistor lengths, it is necessary to normalize the noise pulse width with respect to the duty cycle of the clock signal. The area under these curves decreases with technology scaling which means that the noise immunity is decreasing as technology scales.

4.5.3 Noise Immunity Scaling Trends: Simulation Results

The noise immunity scaling trends of the conventional TSPC latch and two latches implemented with Bobba's technique, Fig 4.40(b), and the proposed technique, Fig 4.40(c), are investigated [76]. Simulation results are obtained using the scalable SPICE Level 3 device model. The test bench for these simulations is shown in subsection 4.2.3 (Fig. 4.21). The noise pulse, characterized by its width and amplitude, is applied at the latch input. Buffering inverters in Fig. 4.21 provide the realistic clock signal. In order to have a real scaling scenario the clock frequency is also scaled. The fanout signal degradation caused by the succeeding stages is simulated by a P-type TSPC latch.

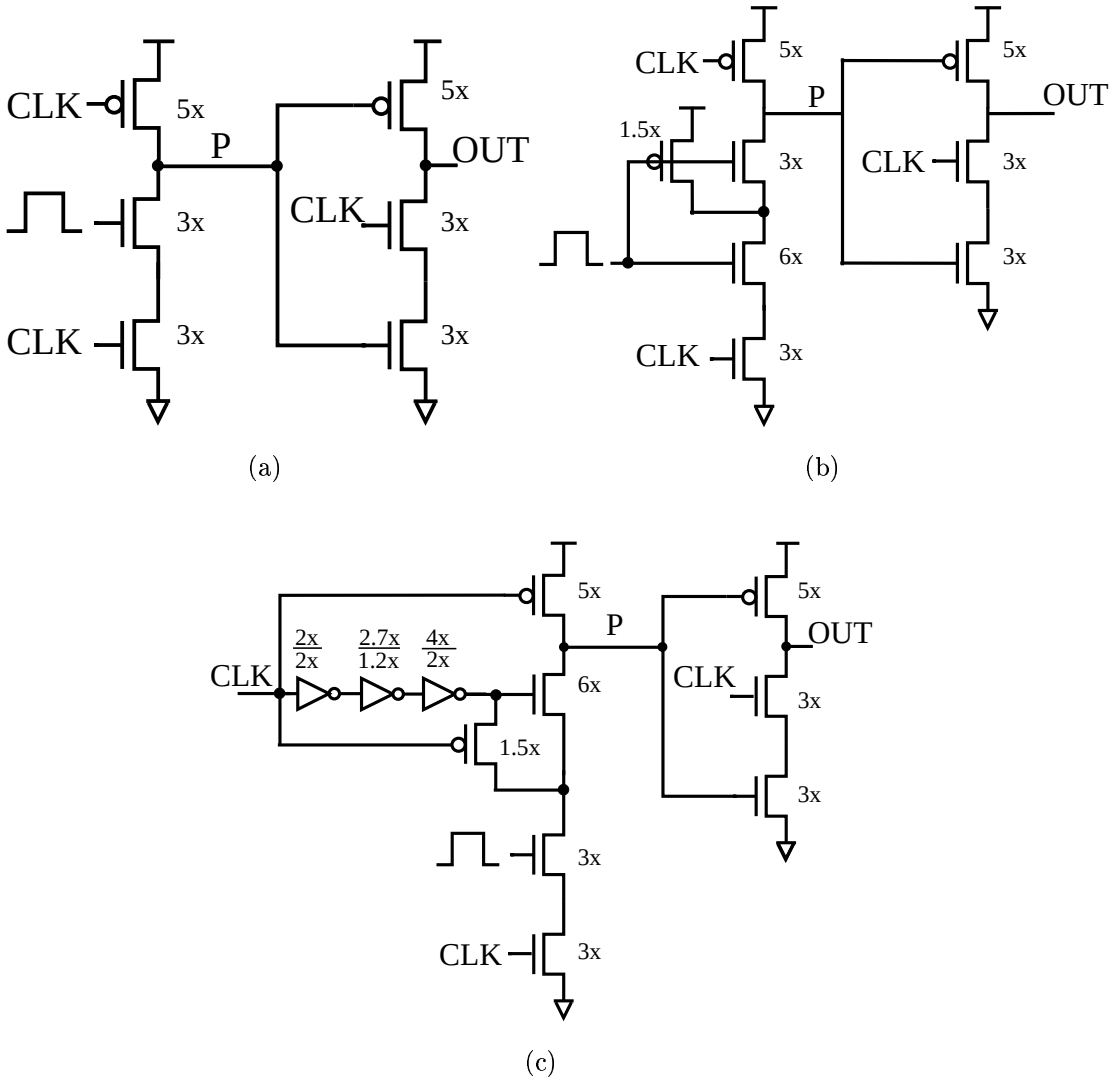


Figure 4.40: TSPC dynamic logic latches: (a) conventional TSPC latch, (b) TSPC latch with Bobba's technique, and (c) TSPC latch with Proposed technique.

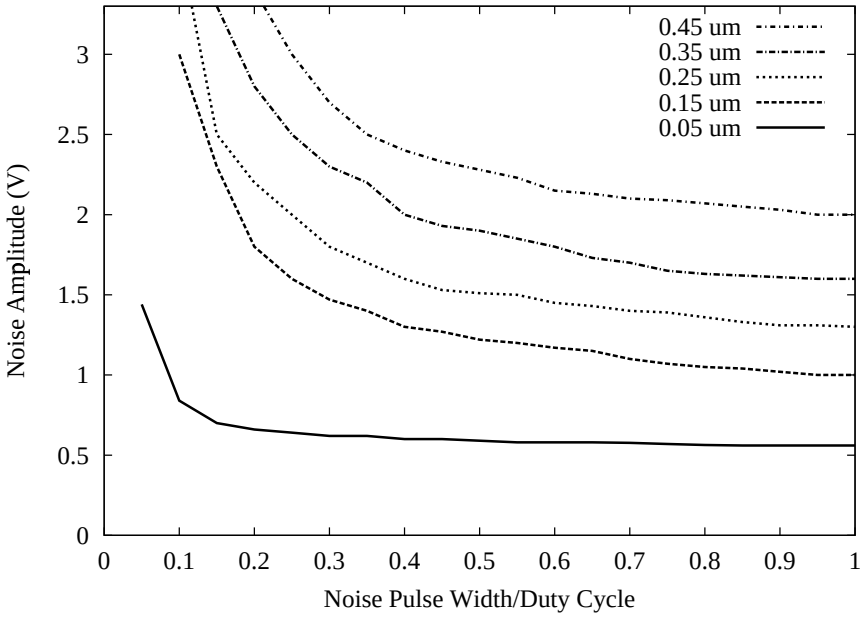


Figure 4.41: Noise immunity curves for the conventional TSPC latch. The noise tolerance decreases with technology scaling.

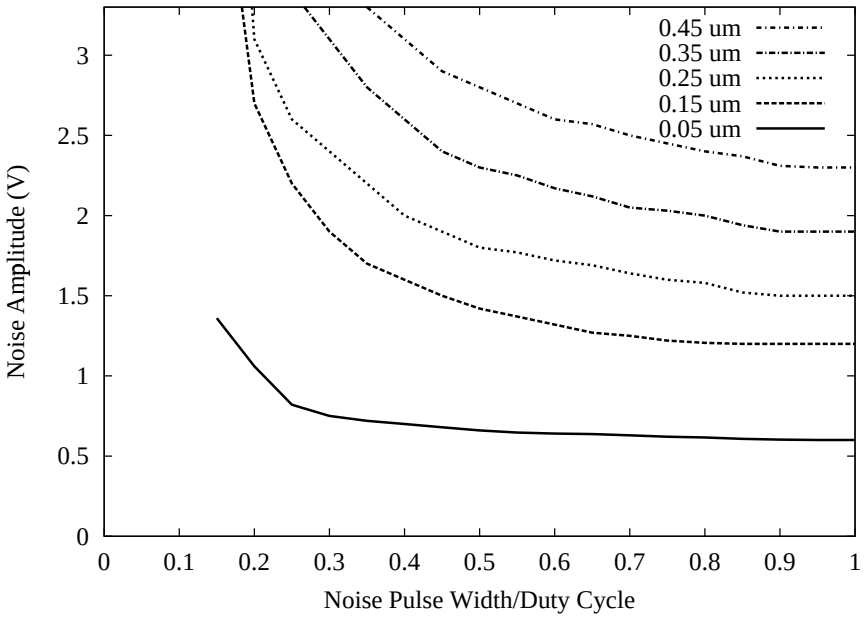


Figure 4.42: Noise immunity curves for the TSPC latch implemented with Bobba's technique.

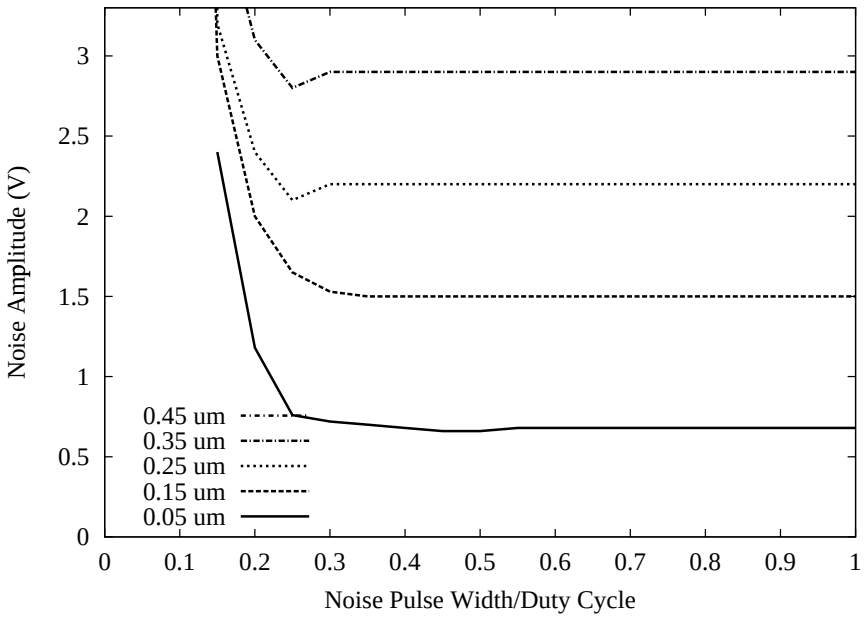


Figure 4.43: Noise immunity curves for the TSPC latch implemented with the proposed technique.

Different noise pulse width and amplitude combinations were applied at the latch inputs. When the voltage level in the dynamic precharge node P was discharged to $V_{dd}/2$ the specific noise pulse width and amplitude were registered to build a noise immunity curve. Figs. 4.41, 4.42 and 4.43 show the noise immunity curves for the latches in Fig. 4.40 taking as a parameter the transistor length. As technology scales noise immunity decreases in all circuits. Thus, if both V_{DD} and V_t are scaling themselves, noise immunity scales the same way because it is proportional to V_{DD} and V_t.

In Fig. 4.44 the noise immunity of the latches under analysis is compared for different transistor lengths. As it can seen, the proposed technique has better noise immunity than Bobba's and conventional dynamic for all technologies considered in the analysis, despite the noise immunity is scaling itself. This result means that the functionality of the proposed technique will be better than existing ones for future technologies. An additional comment about Fig. 4.44 is that the noise tolerance difference between the different latches is reducing itself. This is due to the aggressive voltage supply scaling, which offers less signal swing. Other reason is that the threshold voltage is scaled in a slower fashion than the voltage supply, so, the minimum voltage to turn ON a transistor is becoming a bigger fraction of voltage supply.

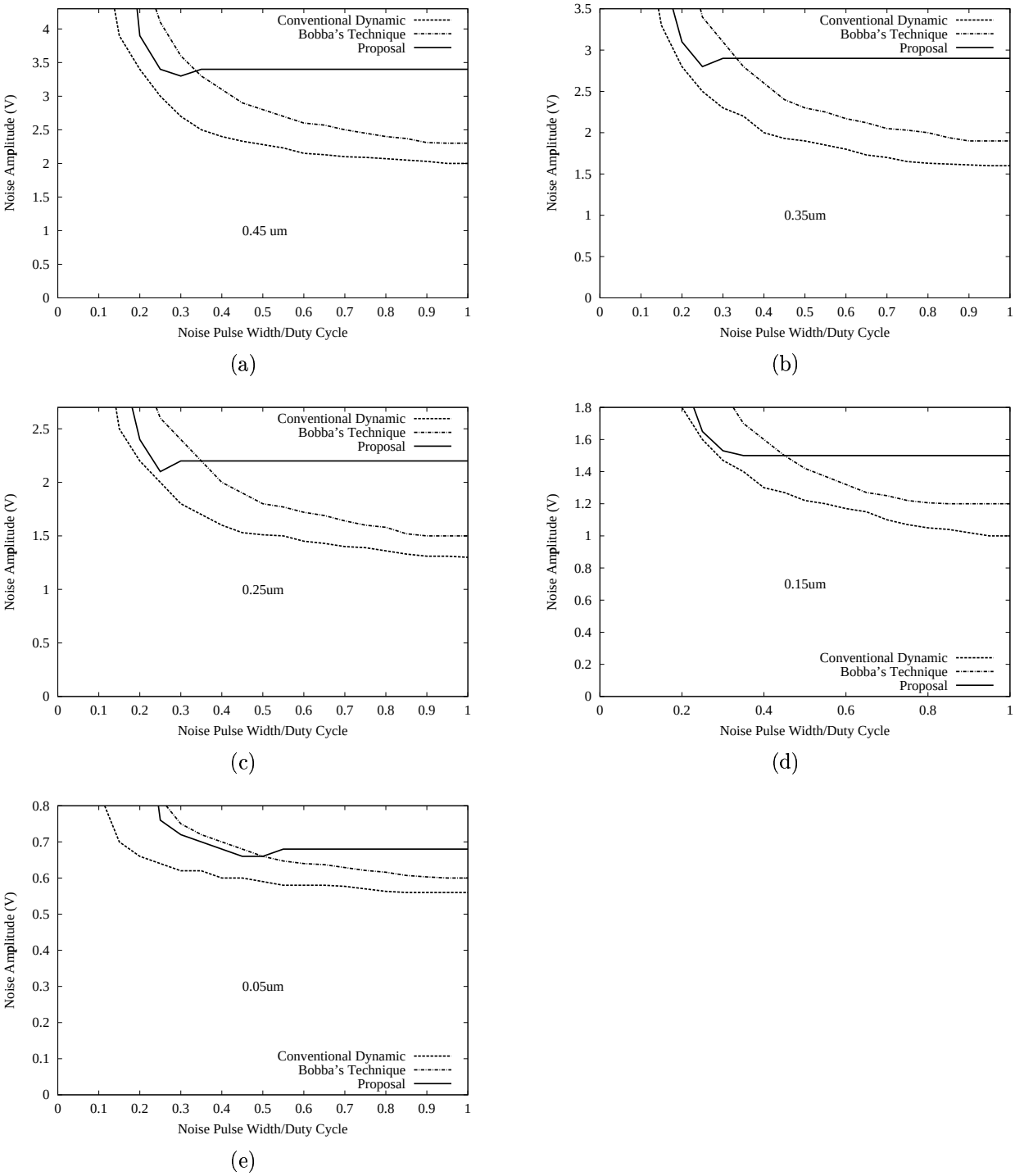


Figure 4.44: Noise immunity curves for the three kind of latches under analysis for several technologies: (a) 0.45 μm, (b) 0.35 μm, (c) 0.25 μm, (d) 0.15 μm, and (e) 0.05 μm.

The performance comparison of the three kind of latches for the different transistor lengths is listed from Table 4.14 to Table 4.18. First, the power consumption penalty of the proposed technique, with respect to the conventional latch, remains almost constant as technology scales. This means that the proposed technique preserves its power penalty as technology scales. In Fig. 4.45 the power scaling trends for the three latches under analysis is shown. Second, the delay penalty, with respect to the conventional latch, is approximately the same for all transistor lengths under analysis. The delay penalty of Bobba's technique is reducing for this particular study case, see Fig. 4.46. Third, regarding noise immunity, the ANTE metric has been obtained from the noise immunity curves shown in Fig. 4.44 for each latch and each transistor length and plotted in Fig. 4.47. As already discussed, the ANTE metric is decreasing with technology scaling. This means less noise tolerance in the logic gates. Nevertheless, the proposed technique always has better ANTE than Bobba's technique and conventional dynamic logic.

Hence, the performance penalty and the improved noise tolerance of the proposed noise tolerant technique seem to be the same for future technologies.

Table 4.14: Performance for TSPC latches for L_{drawn}=0.45μm.

Technique	Power (mW)	$ANTE$ (V^2)	Delay (ps)	$\frac{ANTE}{Delay}$ $(V^2)/ps$
Conv. dynamic	6.5	2.88	124.24	0.023
Bobba's Tech.	6.9	5.07	135.03	0.037
Proposed Tech.	9.4	6.97	134.39	0.051

Table 4.15: Performance for TSPC latches for L_{drawn}=0.35μm.

Technique	Power (mW)	$ANTE$ (V^2)	Delay (ps)	$\frac{ANTE}{Delay}$ $(V^2)/ps$
Conv. dynamic	3.8	1.92	101.34	0.018
Bobba's Tech.	4.0	3.64	117.24	0.031
Proposed Tech.	5.4	4.90	117.80	0.041

Table 4.16: Performance for TSPC latches for L_{drawn}=0.25μm.

Technique	Power (mW)	$ANTE$ (V^2)	Delay (ps)	$\frac{ANTE}{Delay}$ $(V^2)/ps$
Conv. dynamic	1.78	1.26	75.28	0.016
Bobba's Tech.	1.88	2.41	87.32	0.027
Proposed Tech.	2.54	3.20	87.13	0.036

Table 4.17: Performance for TSPC latches for L_{drawn}=0.15μm.

Technique	Power (μW)	$ANTE$ (V^2)	Delay (ps)	$\frac{ANTE}{Delay}$ $(V^2)/ps$
Conv. dynamic	617.5	0.80	51.0	0.015
Bobba's Tech.	667.5	1.35	59.0	0.022
Proposed Tech.	885.6	1.64	64.7	0.025

Table 4.18: Performance for TSPC latches for L_{drawn}=0.05μm.

Technique	Power (μW)	$ANTE$ (V^2)	Delay (ps)	$\frac{ANTE}{Delay}$ $(V^2)/ps$
Conv. dynamic	37.5	0.19	38.3	4.96e-3
Bobba's Tech.	41.1	0.25	44.7	5.59e-3
Proposed Tech.	54.5	0.32	49.0	6.53e-3

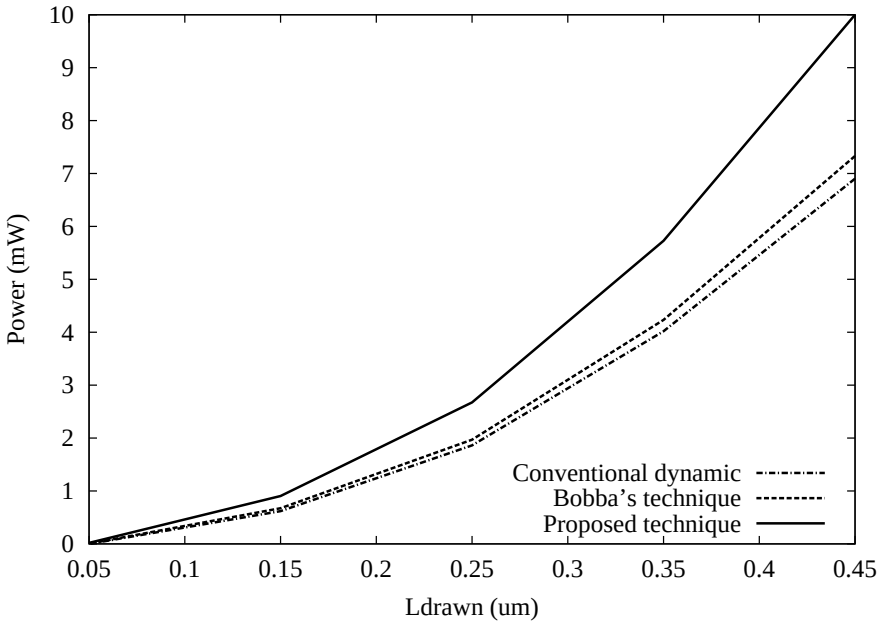


Figure 4.45: Power consumption for different transistor lengths.

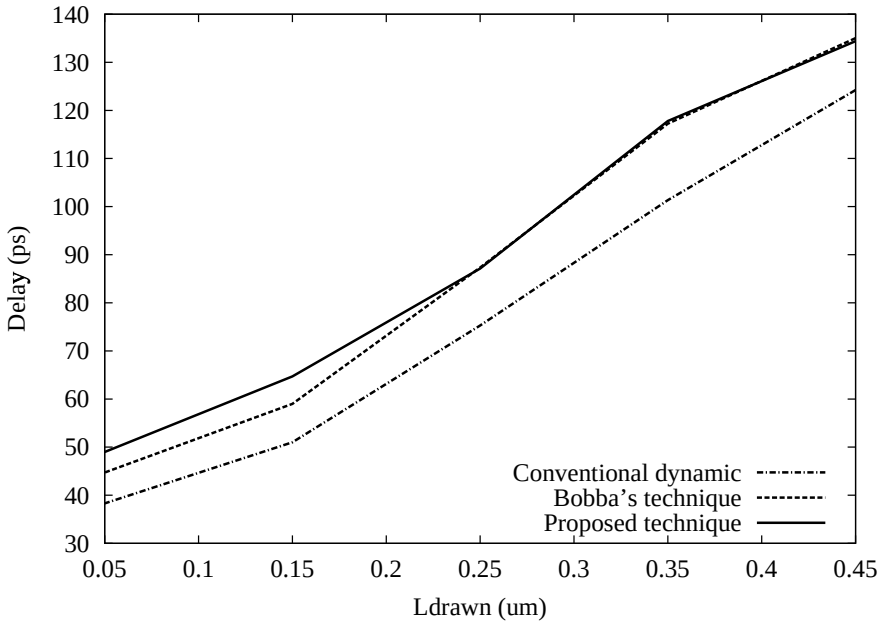


Figure 4.46: Delay of the latches for different transistor lengths.

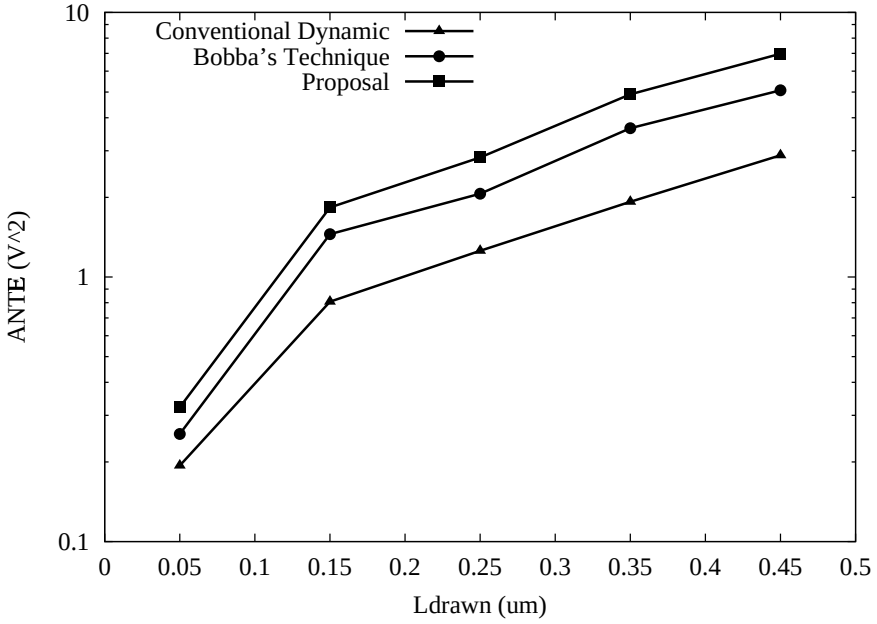


Figure 4.47: ANTE metric for several technologies and latches.

4.6 Further Improvements

In this section a new topology of the proposed noise tolerant technique is presented. This new topology intends to enhance the performance and noise immunity of the logic gates to make the circuits more efficient.

4.6.1 Operation of the Improved proposed technique

Fig. 4.48 shows an improved version of the proposed noise tolerant technique. The transistors in the PDN have been reordered. The transistor M_2, which is controlled by CLK, is placed at the top of the PDN. The N logic is located at the bottom of the PDN and transistors M_P and M_N form a resistive voltage divider in the same fashion as the Inverter technique.

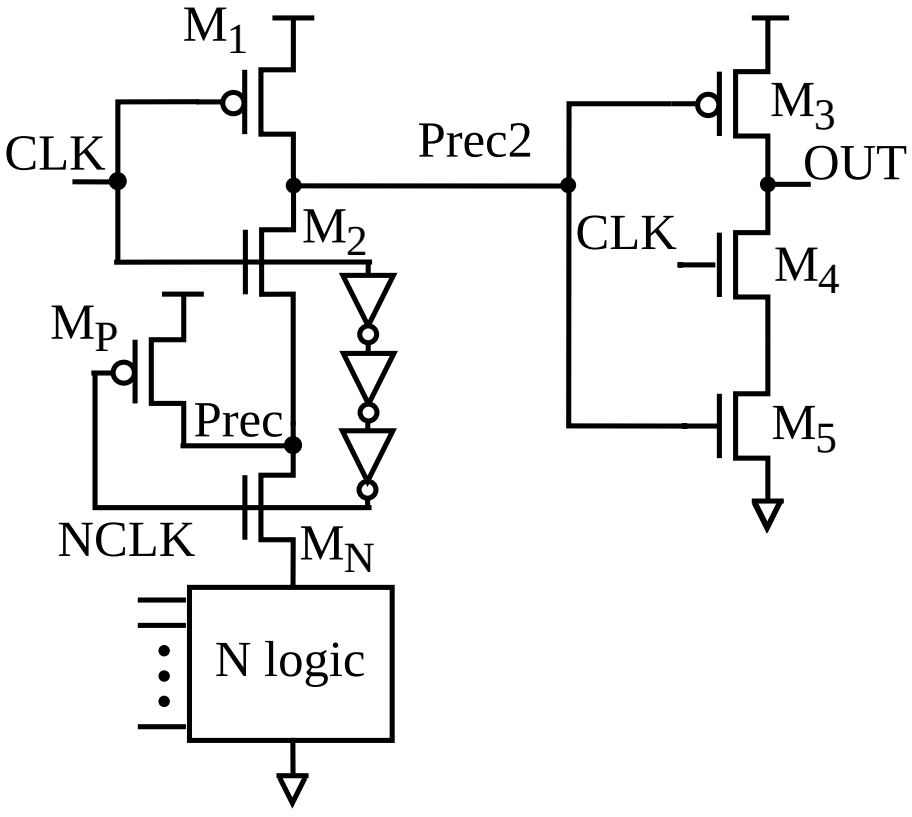


Figure 4.48: Improved proposed technique.

In precharge phase (CLK=0, NCLK=0), *prec2* and *prec* nodes are charged to V_{DD} through

M_1 and M_P transistors, respectively. The output remains in a high impedance state because the *prec2* node is HIGH and CLK is LOW. Consequently, the PDN block is disconnected from the output.

At the beginning of the evaluation phase (CLK=1) NCLK rises to V_{DD} generating a transparency window. The M_P transistor is turned OFF. If the N logic is OFF the *prec2* precharge node is not discharged and the output preserves a LOW logic state or goes LOW. If the N logic is ON the *prec2* node goes LOW and the output preserves a HIGH logic state or rises to V_{DD}. After three inverter delays the NCLK node falls down and the transparency window disappears.

After the transparency window (NCLK=0), the *prec* node rises to V_{DD} because M_P is turned ON by the NCLK signal. M_2 is also ON because NCLK is still HIGH, so, an amount of charge is redistributed from *prec* to *prec2* and the precharge node starts to rise, if it was discharged, immediately after the transparency window. This fact can degrade the HIGH logic level of the output, but with a careful transistor sizing, the logic level at the output is preserved.

4.6.2 Comparisons

The afore mentioned charge redistribution gives additional noise immunity to this technique (the precharge of *prec* node gives noise immunity), because when a noise pulse is trying to discharge the dynamic node, the charge redistribution process counteracts the discharge and the dynamic node rises its logic voltage. In this way, the output have a glitch but preserves its logic state. In Fig. 4.49 three noise pulses are applied to both, the gates implemented with the noise tolerant technique and to the conventional gate. The output of the improved proposed technique restore its logic state and no logic error occurs.

This improvement in the proposed technique preserves the correct operation of logic gates. Fig. 4.50 shows a transient simulation of a 2 input TSPC AND gate implemented with the improved proposed technique. The waveform marked as INPUTS is applied at both gate inputs, so, the output (waveform marked OUTPUT in Fig. 4.50) has the same shape as the inputs. Note that the NCLK signal is HIGH only at the beginning of the evaluation phase.

Placing the N logic block at the bottom of the pull down network makes a pre-discharge of the N logic when all inputs rise before the evaluation phase. This mechanism improves the

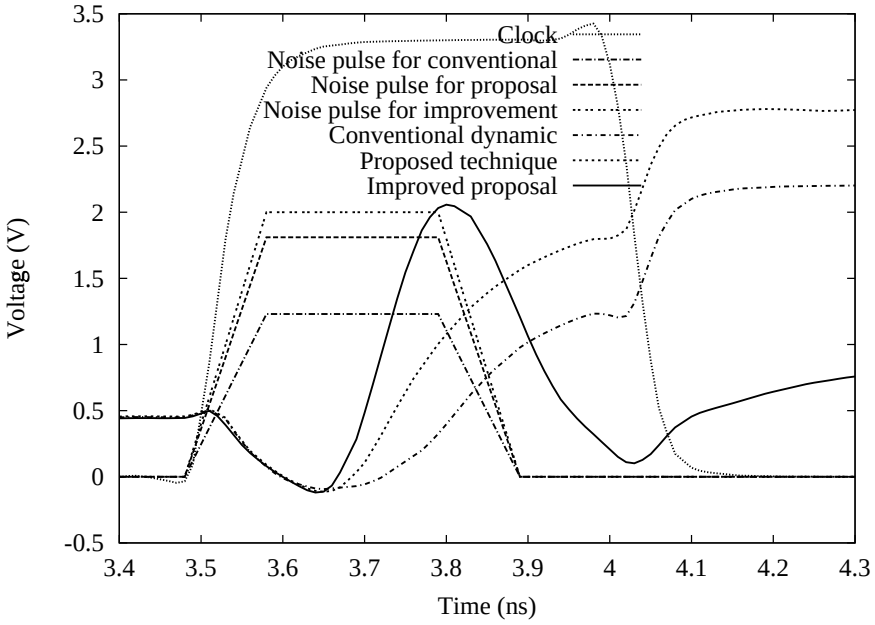


Figure 4.49: Unity Noise Gain from a transient simulation for 2 input TSPC AND gates. In the improved proposed technique the output recovers its logic state after a noise pulse occurs.

delay of the improved proposed technique. In Fig. 4.51 the delay of a 2 input TSPC AND gate is compared with those of the gate implemented with the proposed technique and the improvement. As it can be seen, the delay of the improvement is almost the same as the one of the conventional gate.

Table 4.19 summarizes the performance of the AND gates. The improved proposed technique has slightly more power consumption and better noise immunity (given by the UNG metric) than the original proposed technique and the conventional dynamic. So, the UNG-delay ratio is improved in comparison with the one of the original proposed technique.

Table 4.19: Performance for 2-input TSPC AND gates.

TECHNIQUE	Power (mW)	UNG (V)	Delay (ps)	$\frac{UNG}{Delay}$ (mV/ps)
Conv. dynamic	3.37	1.23	124.82	9.85
Proposed Tech.	3.77	1.81	135.72	13.33
Improved Tech.	3.83	2.00	124.98	16

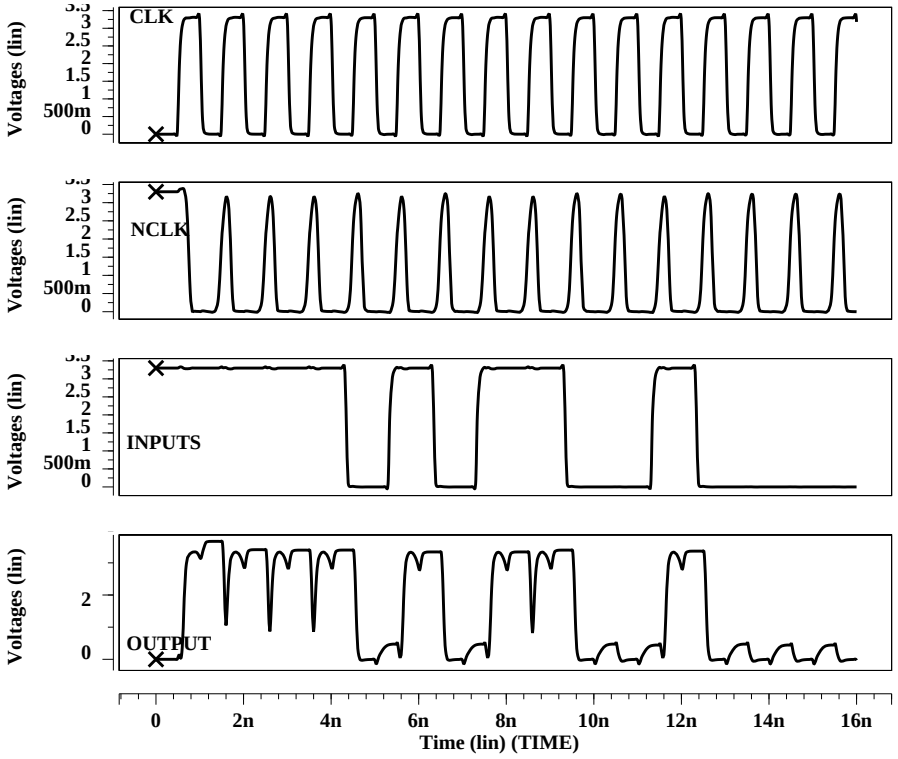


Figure 4.50: Normal operation of the improved proposed technique for a 2 input TSPC AND gates.

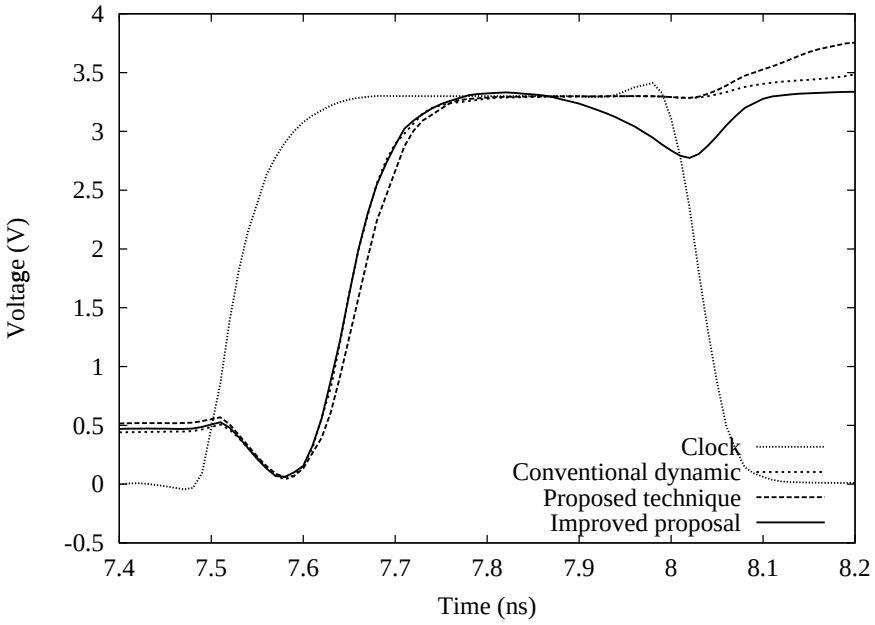


Figure 4.51: Output response for 2 input TSPC AND gates.

4.7 Conclusions

In this chapter a new noise-tolerant dynamic circuit technique suitable for dynamic digital systems was presented. The application of this technique to a conventional dynamic gate like TSPC or Domino is simple as the pull down network that defines the type of gate is not altered. The delay circuitry that defines the transparency window adds 6 extra transistors to the gate. However, this delay circuitry can be shared by two or more gates in the same pipeline stage. If the delay circuitry is not shared, the implementation of the proposed technique adds 8 transistors (6 in the delay circuitry and 2 in the PDN), no matter the fan-in of the gate. These added transistors can seem too much in a TSPC latch (which consists of 9 transistors) because increase the transistor count by 88%. Nevertheless, for a large or wide fan-in gates the extra transistors are a small fraction of the total. For instance, a 16 input TSPC OR gate consists of 21 transistors. Now, the added transistors represent only 21.5 % of the total. Furthermore, if the delay circuitry is shared by two or more gates the transistor increase is less severe.

Two strategies are used by the proposed technique to improve the noise tolerance of dynamic gates: rising the threshold voltage of the gate by precharging an internal node in the

PDN, and isolating the dynamic node from the inputs when the PDN has been evaluated. The combination of these strategies gives to the proposed technique their high noise immunity. The transparency window must be designed in such a way that correct logic operation is assured.

Noise immunity curves and *ANTE*-delay ratio show that this technique improves the noise immunity with less performance degradation than existing noise-tolerant techniques for AND gates and with an acceptable performance degradation for OR gates.

The noise tolerance of dynamic digital circuits with technology scaling has also been investigated. Using an analytical noise immunity model and a reliable scaling scenario, scaling trends for the noise immunity of dynamic digital circuits has been investigated. The main result that arise from this analysis is that dynamic noise margins will be reduced in future technologies mainly due to the supply and threshold voltage scaling. However, the proposed technique will continue being the better choice for noise immunity because preserves its better noise immunity against previously proposed noise immune techniques for several submicron technologies.

Chapter 5
EXPERIMENTAL RESULTS

Circuits with the proposed technique have been designed and fabricated. A 0.35 μm AMS technology was used. Measurements have been carried-out in the circuits.

The organization of this chapter is as follows: first, the test circuit and a noise injection circuit are introduced. Later, the CAD design flow used to design these structures is described. The test circuit performance is further analyzed, normal operation and operation under noise injection are considered.

5.1 The Test Circuit Architecture

In this section the architecture of the test circuit is given. The main scope is to design a test structure, which has been implemented with the proposed technique, which can tolerate the noise pulses injected at a given internal node. The structure under test is a 1-bit carry look-ahead full adder using TSPC dynamic logic in which both, P- and N-blocks are implemented with the proposed technique.

5.1.1 A 1-bit Carry Look-Ahead Full Adder

Adders are the most common arithmetic circuits in digital systems. Adders are main components of multipliers and dividers and also are used to perform subtraction. A full adder adds three

1-bit inputs. Two of the inputs are the bits to be added (denoted x_0 and y_0), and the other input is the carry from the lower significant bit position (denoted C_0), producing a sum bit (denoted s_0) and a carry bit (denoted C_1) as outputs. The truth table for a full adder is shown in Table 5.1.

Table 5.1: Truth table for a full adder.

x_0	y_0	c_0	s_0	c_1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean expression that determines the logic function is shown in equation (5.1).

$$s_0 = x_0 \oplus y_0 \oplus c_0 \tag{5.1}$$
$$c_1 = x_0 \cdot y_0 + x_0 \cdot c_0 + y_0 \cdot c_0$$

Despite there are many implementations of this full adder [38] which have short latency time, it is preferred to implement the full adder in a 4-stage pipeline (see Fig. 5.1) to verify the effectiveness of the proposed technique when P- and N-blocks are pipelined. Furthermore, applying a noise pulse in the second stage of the pipeline, a more realistic logic failure situation can be produced. This concept can be clarified using the full-adder logic diagram shown in Fig. 5.1. The noise pulse is injected at the node marked with an "a" (in the first N-block). A noise pulse with sufficient amplitude and width will generate an undesirable logic transition at the output nodes marked "b" and "d". This failure, depending on the input levels, will propagate through "c", "f" or "e" and finally the outputs "s_0" and "c_1" will show a logic failure. In this way, both the N-blocks and the P-blocks are affected by the noise effects and contribute to measure the overall noise immunity.

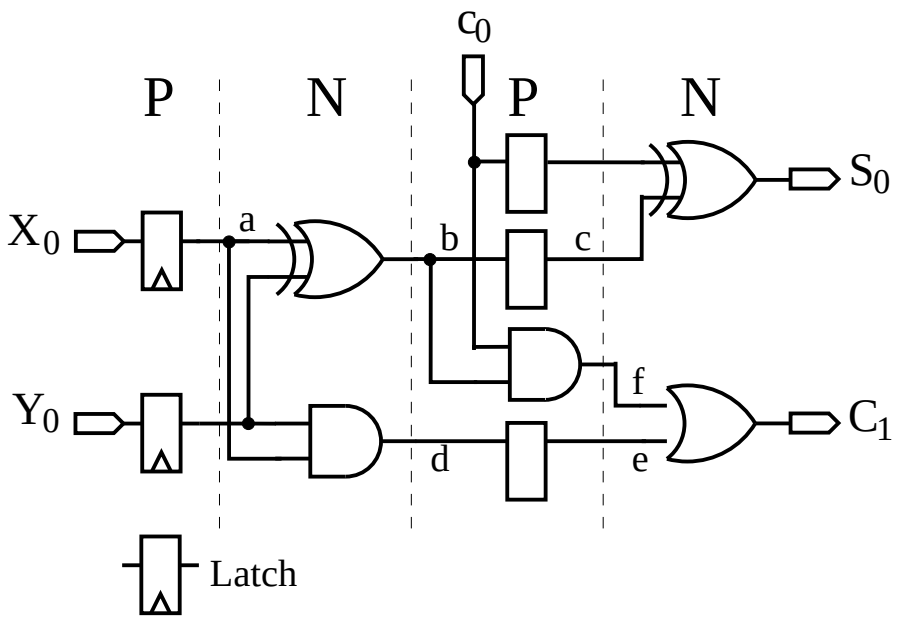


Figure 5.1: Logic diagram of a 1-bit carry look-ahead full adder.

5.1.2 Noise Injection Circuit

Due to the random characteristic of crosstalk noise it is difficult to control the generation and shape of noise pulses by means of a intentional capacitive coupling between two or three interconnections. Instead of that, an easy way to generate glitches in a so called victim node is to use a noise injection circuit (NIC) [62].

The purpose of the NIC is to generate a noise pulse of certain amplitude and width. This to be applied to the selected victim node (the node marked "a" in Fig. 5.1) in the full adder. Fig. 5.2 shows the schematic diagram of the noise injection circuit, which have a tunable delay circuitry made of three inverters. The propagation delay of these inverters and hence the noise pulse duration W_N is controlled by the voltage V_{NW}. This delay circuitry is connected to a two-input NAND gate (node A). A pulse signal is applied to both the delay circuitry and the NAND gate (node T). Consequently, due to the logic function of the NAND gate, an inverted pulse is generated at node C (see Fig. 5.2). The output stage of the NIC is an inverter whose voltage supply V_{NA} is tuned for controlling the amplitude of the noise pulse. When the NIC is triggered the output inverter acts like a static CMOS inverter because the transistor M_g is

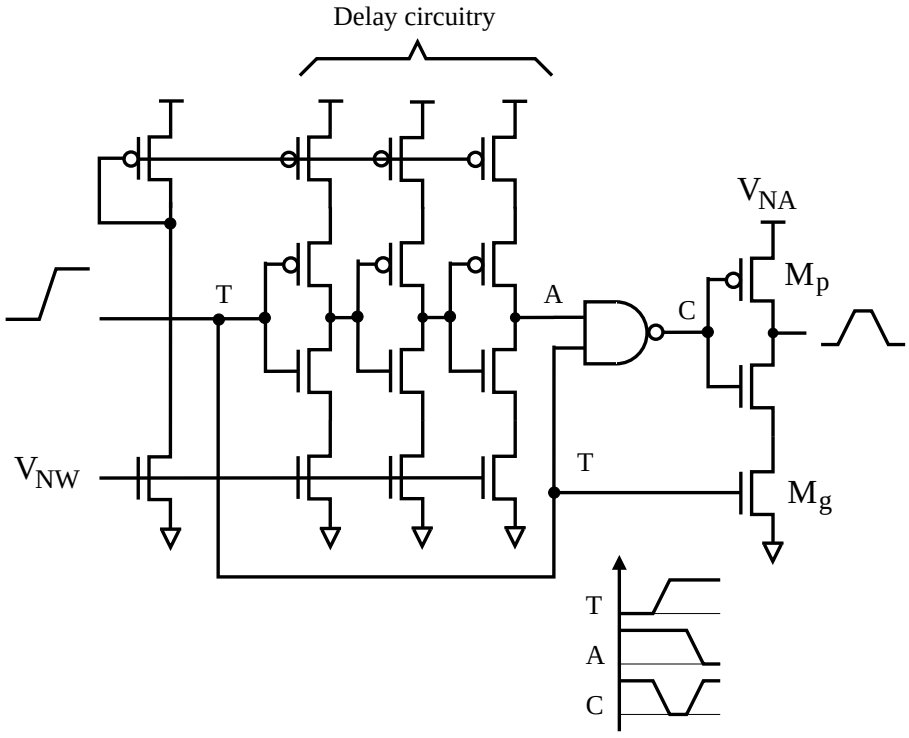


Figure 5.2: Schematic of the noise injection circuit.

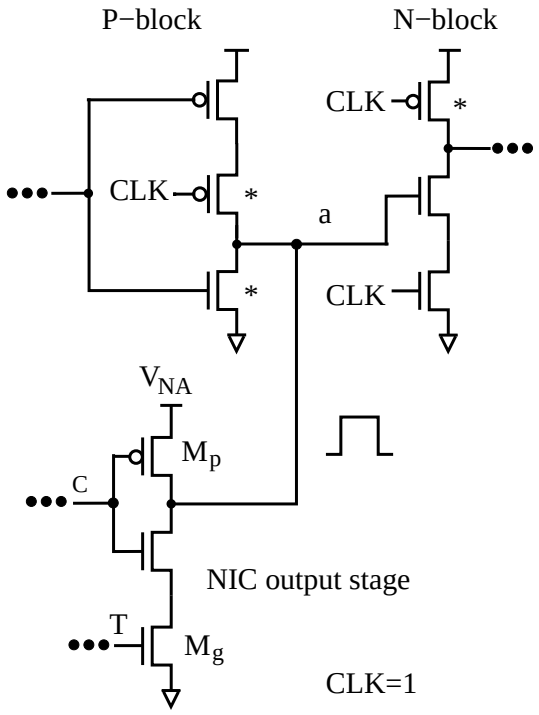


Figure 5.3: Output stage of the noise injection circuit connected to the victim node.

ON. In absence of a pulse signal at the input of the NIC (both nodes T and A are LOW), the transistor M_g is OFF and M_p is OFF too because node C is HIGH. As a consequence, the output of the NIC is in a high-impedance state and there will not be logic mismatch between the NIC and the driver of the victim node (node "a" in Fig. 5.1).

The node "a" in the full adder must be guaranteed to be at a LOW level when the noise pulse is applied. If the clock signal (CLK) is used as the trigger pulse the noise pulse generated at the output in the NIC will be synchronized with the clock, i.e., the noise pulse always appears when the clock is HIGH. This is advantageous because when the clock is HIGH the node "a", which is the output of the P-block, have no direct path to power supply or ground. See Fig. 5.3 where the transistors marked by an asterisk are OFF. In this way, the victim node is floating and logic mismatch can be avoided.

5.2 CAD Design Flow

In this section the CAD design flow of the test circuit is described. In the design process Cadence tools play a key role because all the design process was done using these tools. The CAD design flow used for the design and simulation of the full adder is shown in Fig. 5.4. The design specifications for the circuit must be fixed to the available technology. In this work a 0.35 μm AMS N well, double poly and three metal levels technology was used. Consequently, the design specifications are as follows:

- 0.35 μm AMS N well technology,
- voltage supply=3.3 V,
- maximum clock frequency=800 MHz,
- TSPC dynamic logic style,
- 4 stages pipeline.

After the design specifications were given the schematic capture was done using Virtuoso composer schematic from Cadence. Fig. 5.5 and Fig. 5.6 show the schematic of the full adder and the noise injection circuit, respectively. The transistors were sized to meet the required clock frequency in a recursive process. This means that the schematic of the full adder and the NIC were simulated and transistors resized until the clock frequency was reached. The simulations were made using the Spectre circuit simulator.

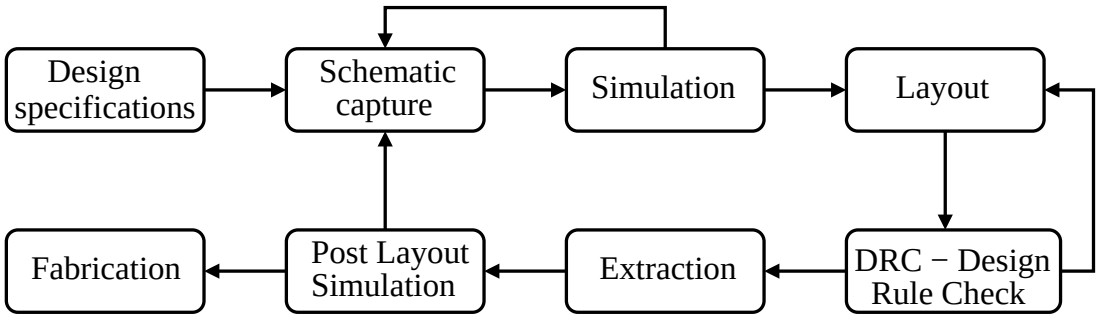


Figure 5.4: The CAD flow used for the design and simulation of the full adder. Cadence tools were used for the entire flow.

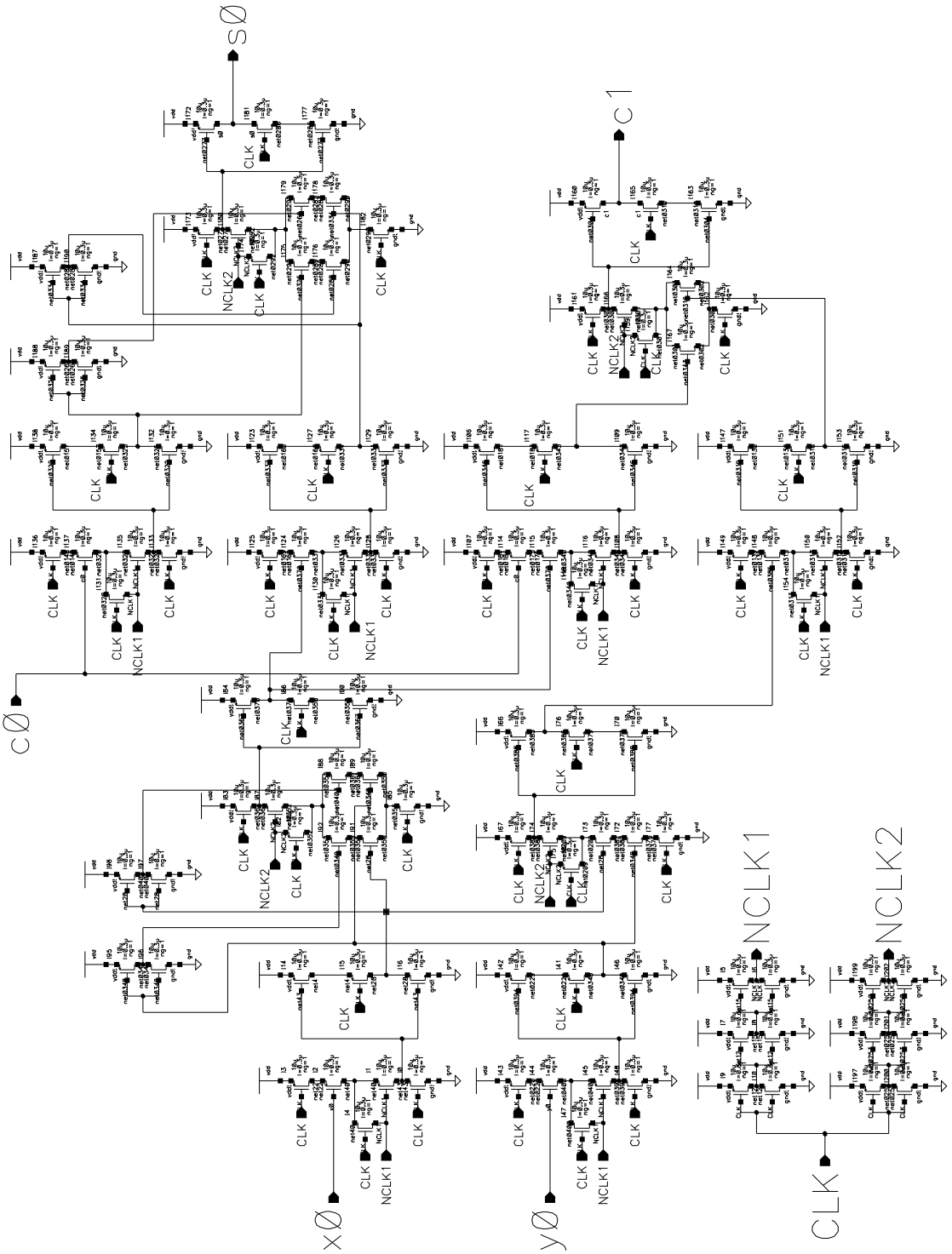


Figure 5.5: Schematic diagram of a 1-bit carry look-ahead full adder.

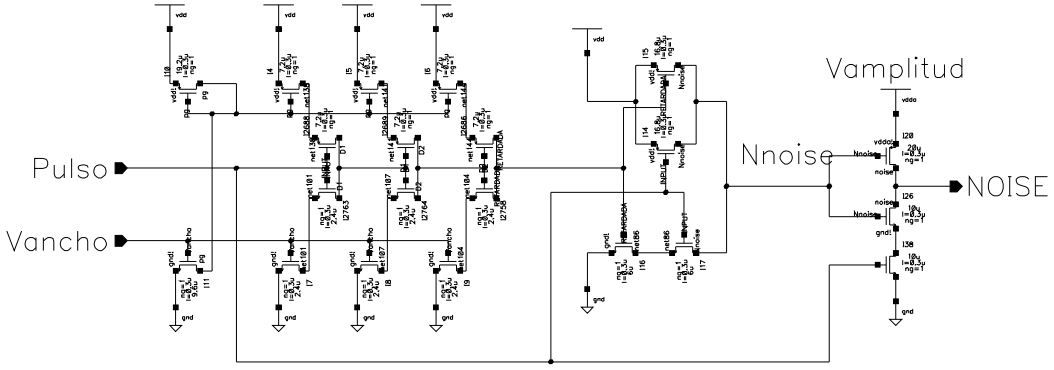


Figure 5.6: Schematic diagram of the noise injection circuit.

Once the test circuit meet the required clock frequency the layout of the transistors was generated directly from the schematic. Next, the transistors were floorplanned and the interconnections were placed. Vertical wires were done with the first metal level, the second metal level was for horizontal wires where power supply and ground lines were included. The third metal level was used to connect the clock-tree and for global wires. The selected layout style was presented by Moraes in [77]. Its main characteristic is that the power supply and ground lines are placed between the PMOS- and NMOS-transistors and the local interconnections are placed outside in a logic gate. Two advantages can be obtained with this layout style:

1. The transistors can be resized if necessary without reaccommodate themselves.

2. Polysilicon lines, which connect the transistor gates, are reduced because both, PMOS and NMOS transistors, are placed closer to each other. This enhance the circuit performance.

Fig. 5.7 shows the full adder and NIC layouts. In the full adder the power lines pass between and over the PMOS and NMOS transistors, and the local connections are below the NMOS transistors and over the PMOS transistors, as stated above. On the other side, the layout of the NIC has a classic style. The NIC is laid-out together with the full adder to avoid a long interconnection which may imply an amplitude degradation in the noise pulse.

During the layout design process the Design Rule Checker (DRC) was used to verify that there were no design rules violations in the layout. Next, the full adder layout was extracted in order to get all the parasitic capacitances.

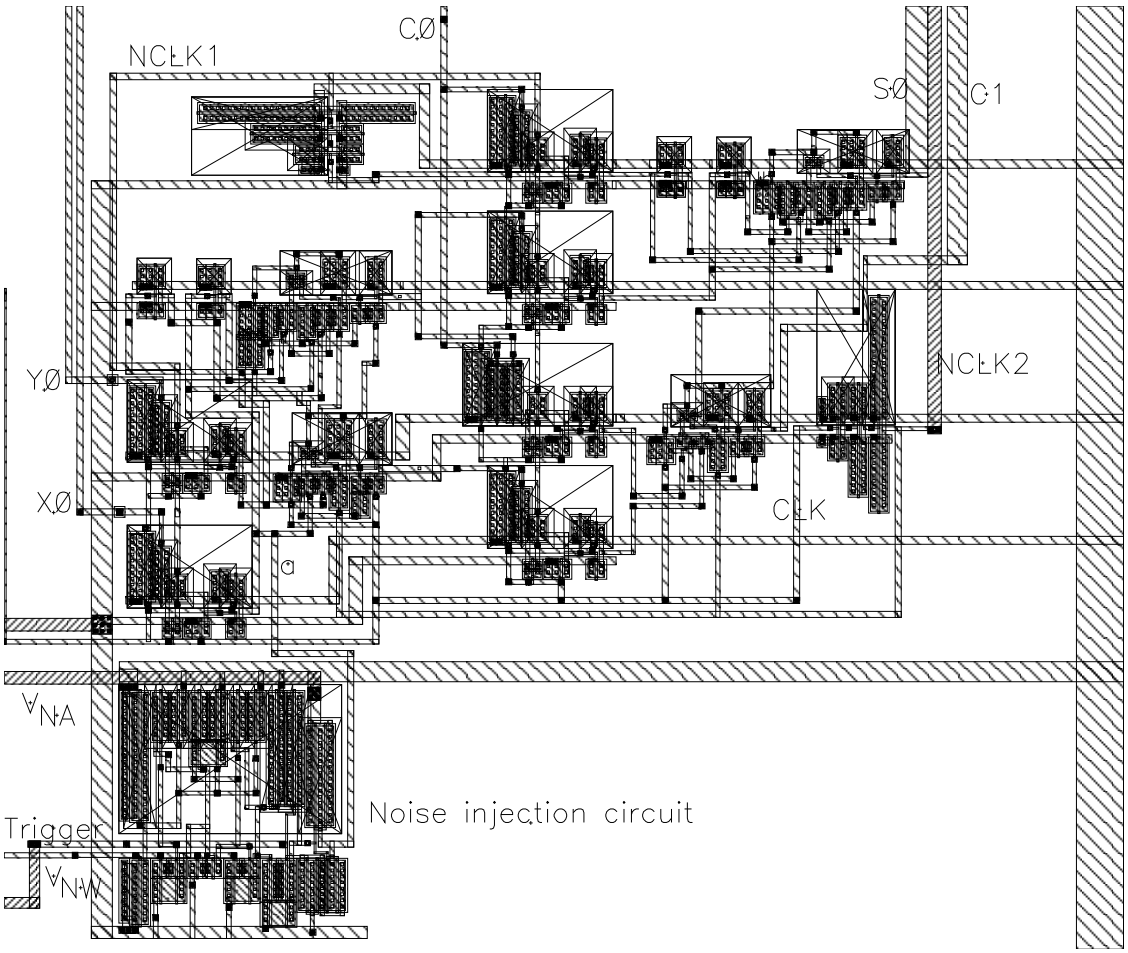


Figure 5.7: Final layout of the test circuit.

One important design parameter is the transparency window size of the test circuit. Whether due to process variations this window is reduced the test circuit could not operate properly. To ensure that process variations do not affect the transparency window size, a Montecarlo analysis was performed to the extracted layout of the full adder. The set of transistor parameters that was varied is: the threshold voltage, mobility, overlap capacitances, gate oxide thickness, zero-bias sidewall bulk junction capacitance and zero-bias gate-edge sidewall bulk junction capacitance. In Fig. 5.8 the transparency window size variations for 40 iterations is shown.

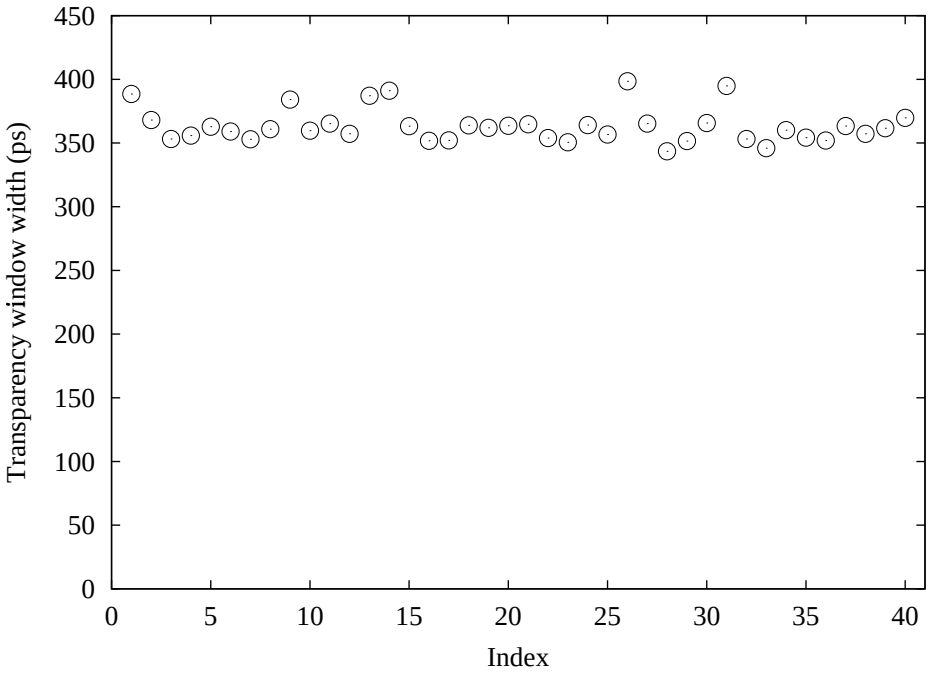


Figure 5.8: A Montecarlo analysis shows that the transparency window width is robust to process variations.

By using Spectre from Cadence, the extracted layout was simulated to verify the correct functioning of the full adder and the NIC when parasitic capacitances were included. In normal operation (without noise injection), the full adder works correctly at a clock frequency of f_{CLK}=500 MHz as it can be seen in Fig. 5.9. A binary counter pulse pattern was applied at the inputs (X_0, Y_0 and C_0). After the latency time of the full adder, which is two clock cycles, the corresponding sum (S_0) and carry out (C_1) were generated as shown in Fig. 5.9.

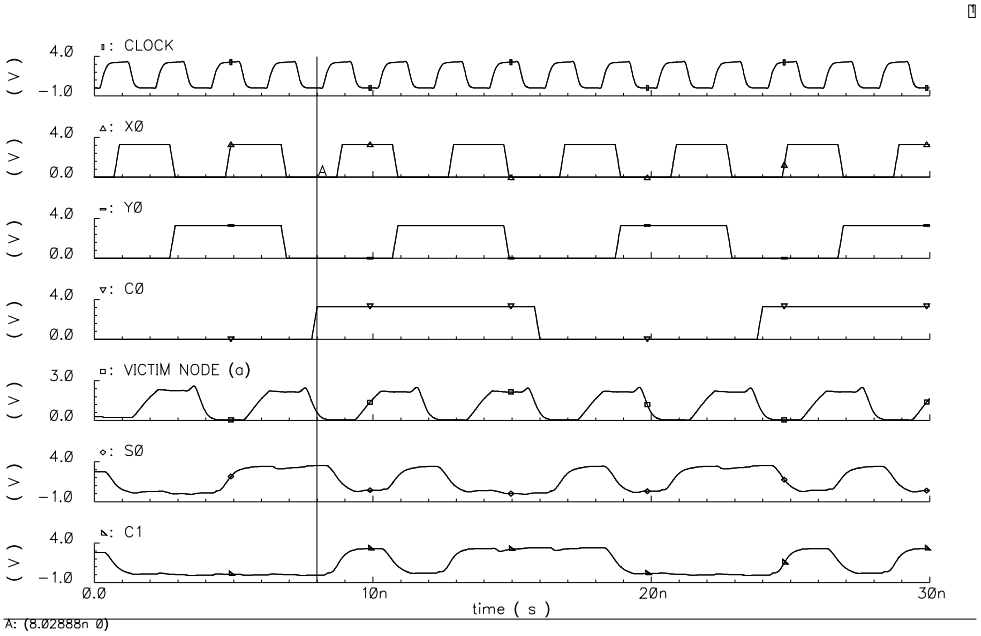


Figure 5.9: Simulation results of the full adder including parasitic capacitances. The NIC is OFF and no noise pulses are injected into the full adder.

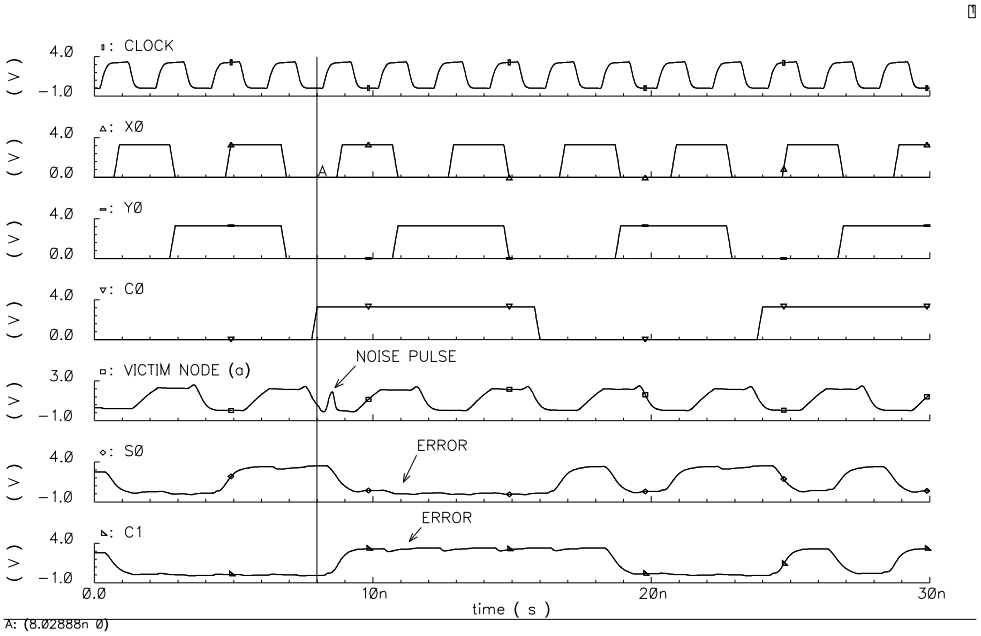


Figure 5.10: when a noise pulse is applied into the full adder a logic failure occurs one clock cycle later.

The operation of the full adder when a noise pulse is applied at victim node "a" is now analyzed. The same binary counter pulse pattern is used at the inputs of the full adder to compare the outputs with those of the normal operation. During the evaluation of the N-blocks, at 8.5 ns, the victim node "a" is LOW and the noise pulse is injected, see Fig. 5.10. The injected noise pulse causes a logic failure that propagates through the subsequent blocks of the full adder and one clock cycle later (at 11 ns) the sum (S_0) and carry out (C_1) signals show an incorrect logic state. S_0 goes HIGH and C_1 goes LOW at 11 ns but they remain unchanged due to the noise pulse.

5.3 Test Circuit Performance

After the post-layout simulation of the full adder, the test chip was fabricated using an AMS 0.35 μm technology. Dices were packaged in a 68 pins JLCC package. The test circuit was fabricated together with other projects. A micrograph of the test circuit is shown in Fig. 5.11.

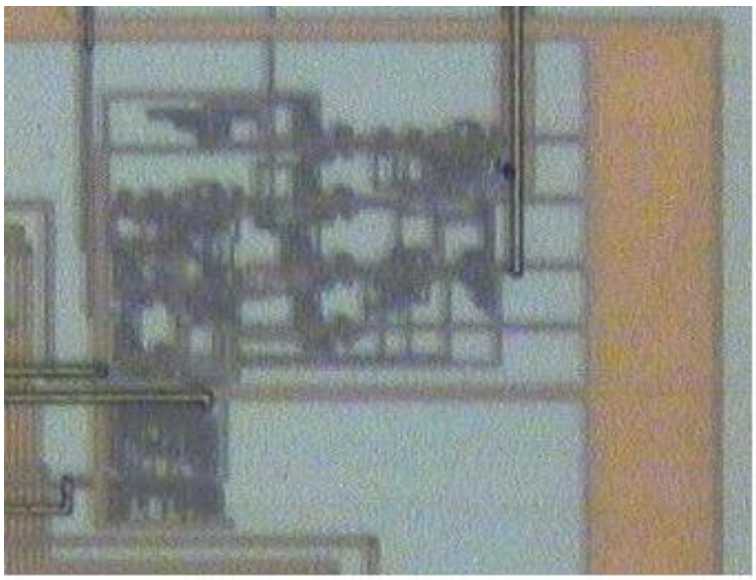


Figure 5.11: Test circuit micrograph.

Before testing for the correct operation and the improved noise immunity of the full adder it is necessary to have a test set-up. A Printed Circuit Board (PCB) was fabricated to mount the test chip, and to have the supply and data connections. The PCB layout is shown in Fig.

5.12.

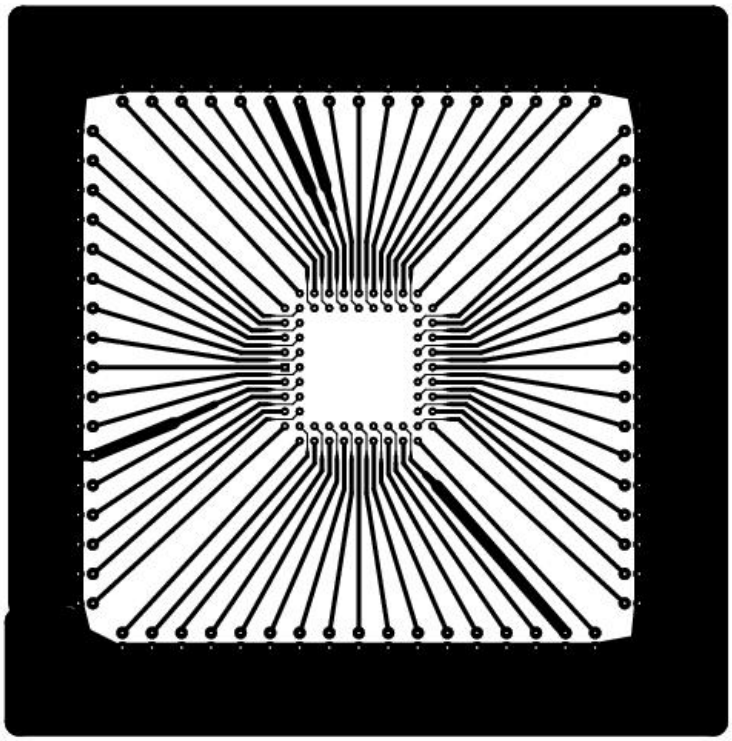


Figure 5.12: Printed circuit board layout used to mount the test chip.

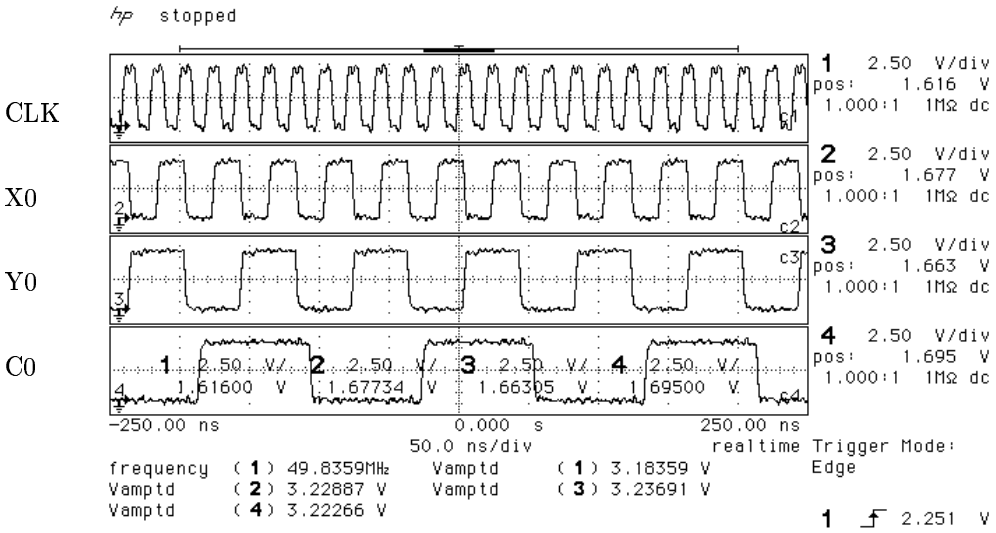
We used two data generators and one oscilloscope to test the circuit. The first data generator was used to generate clock signals with frequency up to 200 MHz. The second data generator (model Sony DG2020A) was used to generate the full adder inputs (X0, Y0 and C0) and operates up to 100 MHz. In this data generator several input patterns can be programmed, this is useful to test the circuit under several input conditions. The oscilloscope (model HP 5050A) operates up to 500 MHz.

5.3.1 Normal Operation of the Test Circuit

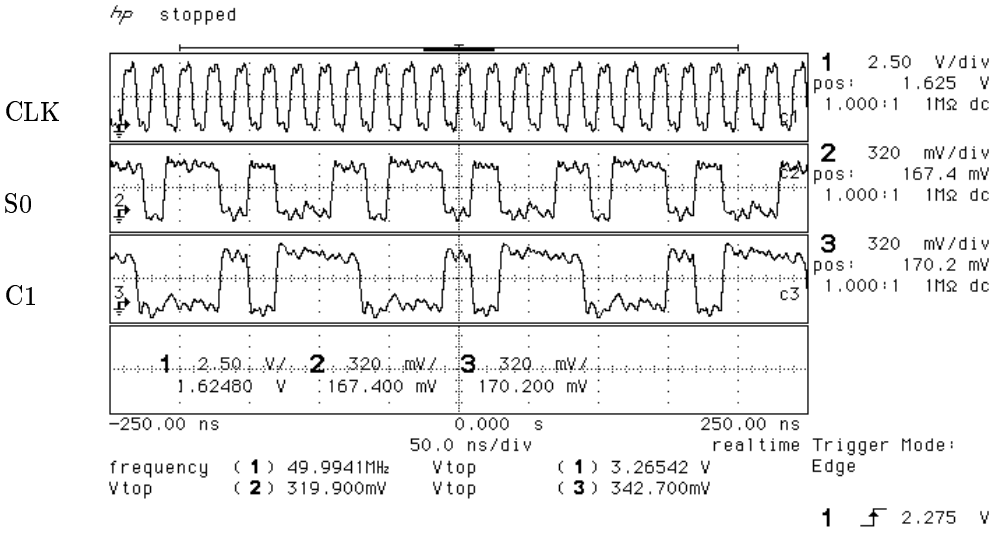
Several input patterns at different clock frequencies were used to test the functionality of the full adder when the NIC is disabled to avoid noise pulse injection. In the following figures time-domain operation of the full adder is shown and the signal waveforms can be related with the full adder logic diagram shown in Fig. 5.1. $X0$, $Y0$ and $C0$ are the inputs and $S0$ and $C1$ are

the outputs, which are indicated at the left of the figures.

The input signals in Fig. 5.13(a), are a binary counter pulse pattern as that used in Fig. 5.9. The clock frequency was f_{CLK}=50 MHz and the voltage supply was V_{DD}=3.3 V. There was no need to use oscilloscope probes with attenuation to measure the input waveforms, so, the probes to measure the full adder inputs were coaxial cables with resistance of 50Ω. On the other side, to measure the full adder outputs it was necessary to use attenuated probes (with attenuation factor 10:1) in order to reduce the noise disturbances. Although the attenuated probes, the resulting sum and carry out waveforms had overshoots and undershoots when measured. This signal degradation is due to the transmission line problem that occurs in the chip to oscilloscope path [78]. The impedance mismatch between the PCB and the oscilloscope probes generate signal reflections and consequently, the shoots. Fortunately, these ripples are not drastic and the output waveforms preserve their shape, see Fig. 5.13(b). The sum and carry out waveforms are equal to the waveforms presented in simulations (see Fig. 5.9), this fact verifies that the proposed noise tolerant dynamic circuit technique allows the correct operation of the gates.



(a)



(b)

Figure 5.13: (a) Binary counter pattern inputs to the full adder, and (b) full adder outputs. f_{CLK}=50 MHz, V_{DD}=3.3 V.

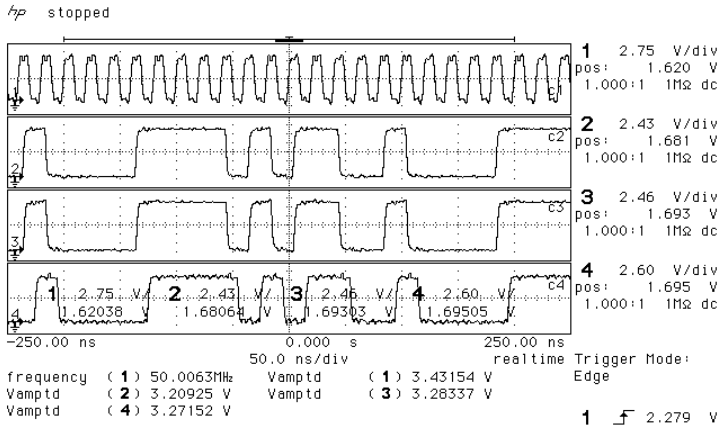
In order to check the operation of the test circuit with other input pattern a pseudo-random pattern was generated with the DG2020A and applied to the full adder inputs using a clock frequency of f_{CLK}=50 MHz and a voltage supply V_{DD}=3.3 V, see Fig. 5.14(a). Due to the test circuit latency, the sum and carry-out are generated two clock cycles later with the same pattern as the inputs [see Fig. 5.14(b)]. The outputs have similar patterns as the inputs because the same pseudo-random sequence is applied to $X0$, $Y0$ and $C0$ and consequently, only a zero or three are generated at the outputs.

CLK

X0

Y0

C0

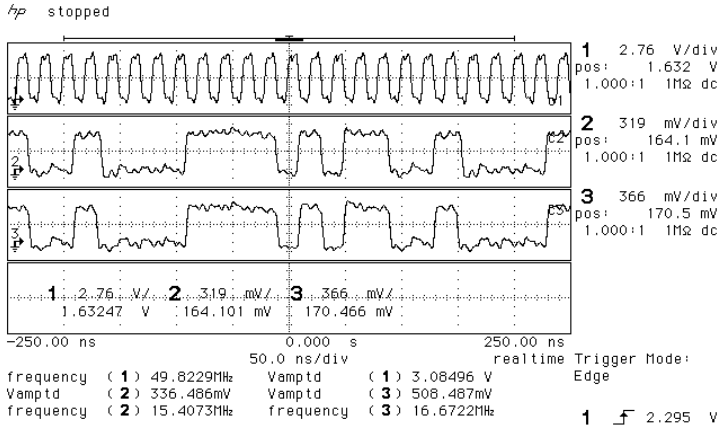


(a)

CLK

S0

C1



(b)

Figure 5.14: (a) Pseudo random inputs to the full adder, and (b) full adder outputs. f_{CLK}=50 MHz, V_{DD}=3.3 V.

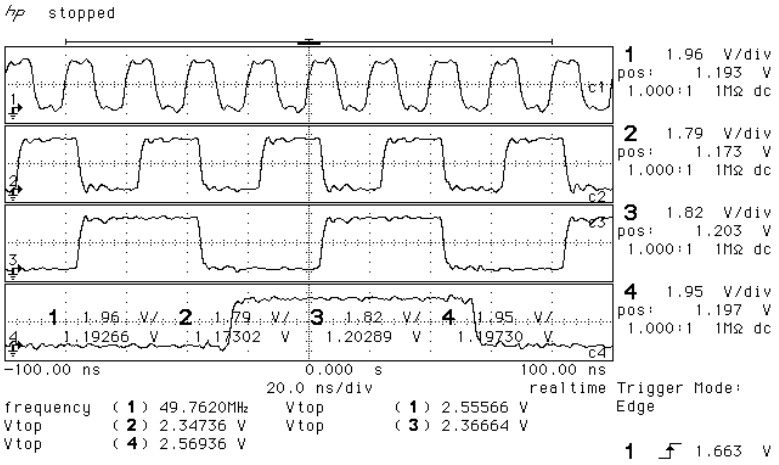
In order to verify the minimum voltage at which the test circuit can operate the power supply was lowered until a logic failure was reached. The minimum voltage supply is 2.4 V as it can be seen in Fig. 5.15(a) where the inputs are depicted and their amplitude is indicated. Fig. 5.15(b) shows that the correct output pattern is produced.

CLK

X0

Y0

C0

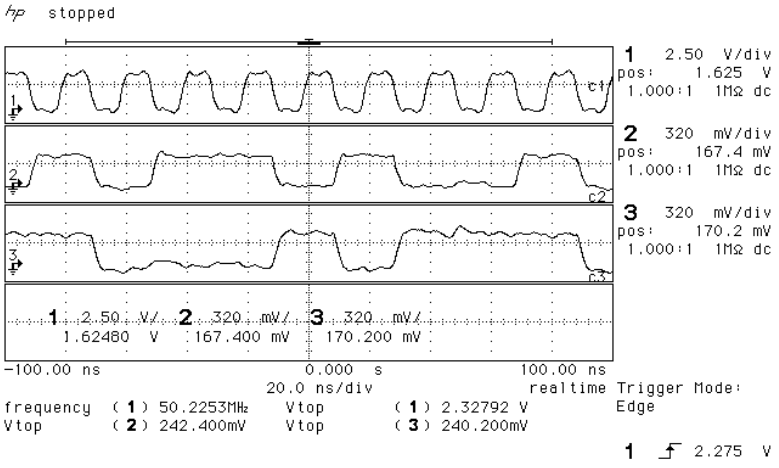


(a)

CLK

S0

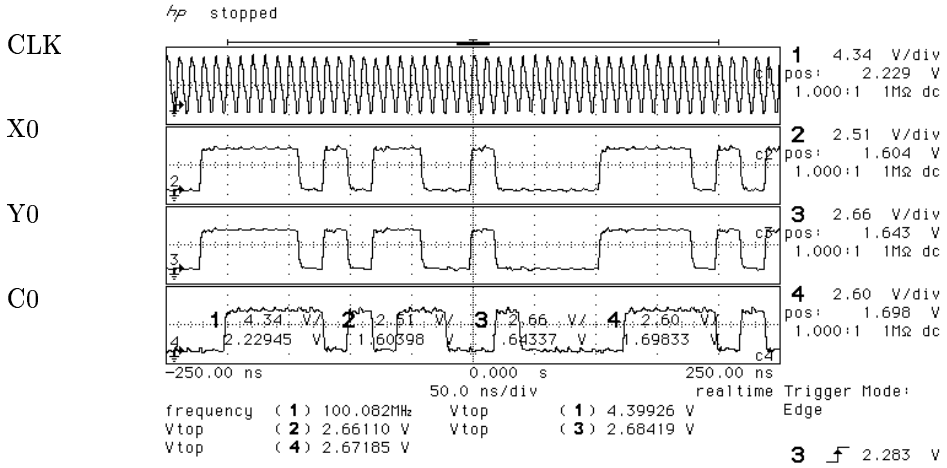
C1



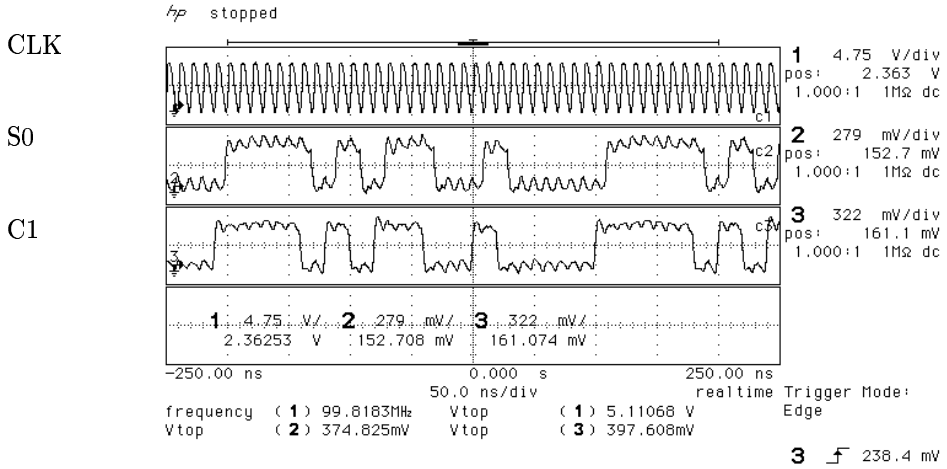
(b)

Figure 5.15: (a) Binary counter pattern inputs to the full adder, and (b) full adder outputs. f_{CLK}=50 MHz, V_{DD}=2.4 V.

The clock frequency was increased to 100 MHz and the pseudo-random sequence was applied to the inputs, see Fig. 5.16(a). The full adder works properly as it can be seen in Fig. 5.16(b).



(a)



(b)

Figure 5.16: (a) Pseudo random inputs to the full adder, and (b) full adder outputs. f_{CLK}=100 MHz, V_{DD}=3.3 V.

At a clock frequency of f_{CLK}=200 MHz the test circuit has a correct operation and the rise and fall times of the outputs are not degraded. Fig. 5.17 shows the sum and carry-out with a pseudo-random sequence at f_{CLK}=200 MHz.

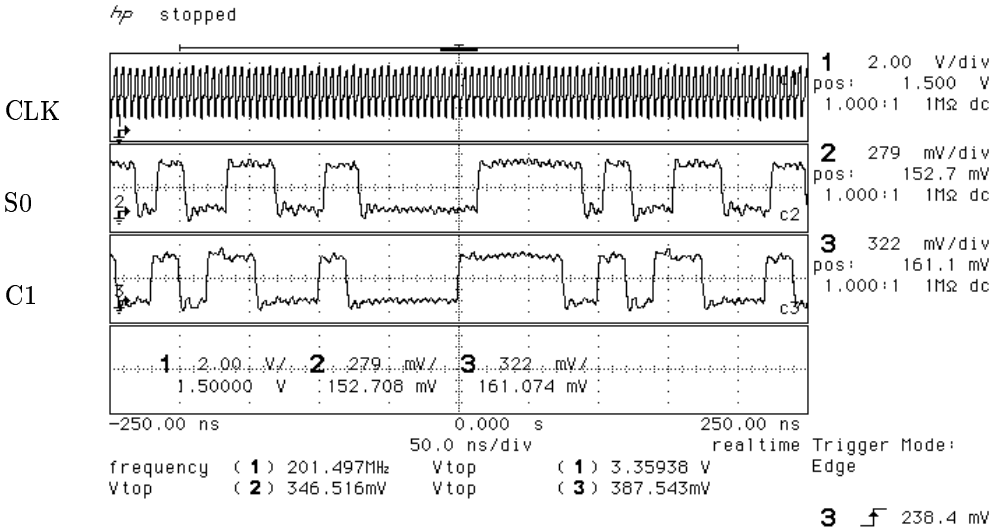


Figure 5.17: Full adder outputs with a pseudo-random sequence for f_{CLK}=200 MHz and V_{DD}=3.3V.

5.3.2 Operation of the Test Circuit Under Noise injection

When a noise pulse with enough amplitude and width to generate a logic failure is applied to the victim node of the test circuit (the node marked "a" in Fig. 5.1), a logic error appears at the outputs, see Fig. 5.18. In this figure, the output waveforms of the full adder when a binary counter pattern is applied at the inputs are shown. When the noise pulse is injected, an incorrect logic level appears at the outputs (marked as "ERROR" in Fig. 5.18).

5.3.3 Noise Immunity of the Test Circuit

To measure the noise immunity of the test circuit the clock frequency is set at f_{CLK}=200 MHz and the inputs are adjusted at a fixed logic level as indicated in Table 5.2. With these logic levels the victim node "a" is "0", and no logic level incompatibility is produced when a noise pulse is applied. The resulting sum S_0 is "1" and the carry out C_1 is "0".

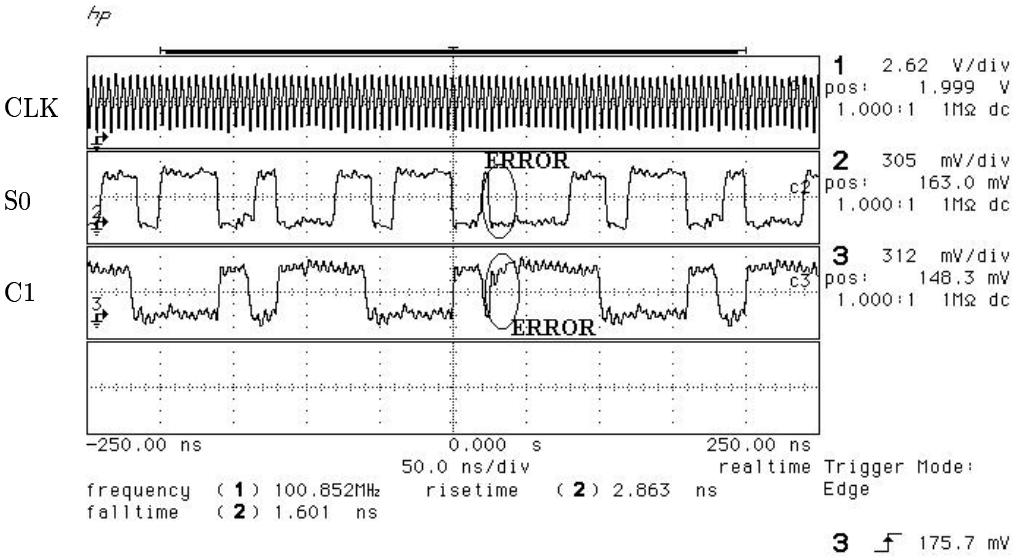


Figure 5.18: When a noise pulse is applied into the full adder a logic error appears at the outputs.

Thus, the NIC is triggered with the clock signal in order to have a noise pulse every time the clock is HIGH (the evaluation phase for N-blocks). The voltage V_{NW} and the voltage V_{NA} in the NIC are adjusted to change the width and amplitude of the noise pulse until a logic failure is obtained at the outputs of the full adder, this means that S_0 changes from "1" to "0" and C_1 changes from "0" to "1". The corresponding noise pulse width and amplitude are incorporated in a width-amplitude graph to build the noise immunity curve.

Table 5.2: Logic levels at the inputs of the test circuit to measure noise immunity.

DATA	LOGIC LEVEL
X_0	LOW
Y_0	HIGH
C_0	LOW

This process is repeated until the noise immunity curve is completed. Fig. 5.19 shows three experimentally measured noise immunity curves for three different chips. These curves are compared with the simulated noise immunity curve of the same test circuit as well as the noise immunity curve for a conventional TSPC full adder. The increment in noise immunity is evident for the full adder implemented with the proposed technique, as its noise immunity curves

are over that of the conventional full adder. Note that the simulated and experimental noise immunity curves of the noise immune full adder agree quite well. Furthermore, these curves become almost constant from a pulse width of W_n=0.4 ns. This is because the transparency window was designed to have a width of 370 ps (see Fig. 5.8), and after this time any noise pulse has no effect on the output of the gate.

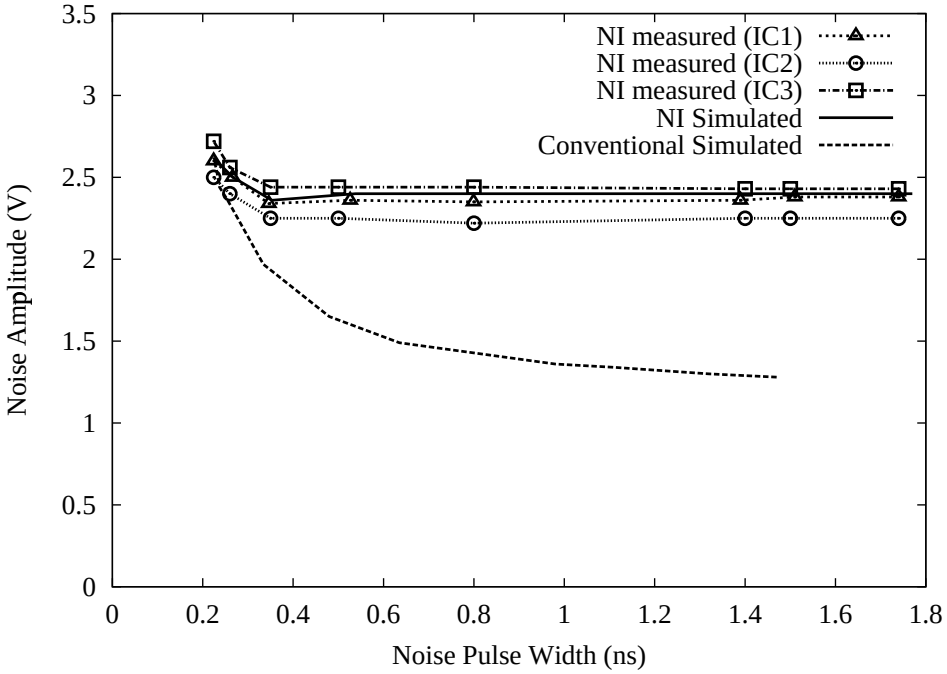


Figure 5.19: Experimentally measured noise immunity curve for the noise-tolerant adder and simulated noise immunity curve for the conventional adder.

The average ANTE metric is obtained from the three experimental noise immunity curves to compare the noise immunities of the full adder implemented with the proposed technique and the conventional one in a quantitative way, see Table 5.3. The noise immune full adder improves the noise immunity 2.95 times over the conventional TSPC full adder.

Table 5.3: Average Noise Threshold Energy (ANTE) from the test circuit and the conventional full adder.

TEST CIRCUIT	ANTE ($V^2 - ns$)
Conventional TSPC full adder	1.63 (simulated)
Noise immune full adder	4.82 (measured)

5.4 Conclusions

In this chapter experimental results, which confirm that the proposed noise tolerant technique improves the noise tolerance of dynamic circuits, were shown. The use of a CAD design flow where Cadence tools were of great importance a test circuit was fabricated in a 0.35 μm AMS technology. This test circuit consists of a pipelined 1-bit full adder and a noise injection circuit (NIC).

The noise injection circuit was effective to inject noise pulses into the full adder. The output stage of the noise injection circuit avoids static power consumption in normal operation. This is because it was always in a high impedance state except in the case where a noise pulse was injected. For normal operation the full adder was tested up to 200 MHz. Several data input patterns was used and the full adder had a correct operation (the sum was right).

In order to acquire noise immunity curves from the test circuit the inputs were set constant and the victim node was assured to be 0. Noise immunity curves were obtained injecting noise pulses with variable amplitude and width into the victim node of the test circuit. These noise immunity curves have better noise immunity for the full adder implemented with the new technique than the noise immunity curves for a conventional dynamic full adder. This test circuit was useful to verify that the new noise tolerant dynamic circuit technique can be implemented in a pipelined circuit increasing its noise immunity with a slight performance penalty.

Chapter 6
CONCLUSIONS

The continuous technology scaling trends have made possible an increment of integration in a single chip. Because this, the complexity of current circuits has significantly increased. Downsizing of devices decreases the switching time and higher-speed operation of circuits is reached. Voltage supply is scaled to reduce power consumption, especially in portable and wireless systems with very low power budgets. Threshold voltage also needs to be scaled to preserve the performance of the circuits. However, these improvements come at expense of higher noise levels at the interconnections and reduced noise tolerance in the circuits. In this way, noise tolerant dynamic digital circuit techniques are needed to alleviate signal integrity challenges in deep-submicron circuits. This work address this challenge with the design and implementation of noise tolerant dynamic digital circuit techniques that are efficient to avoid disastrous effects on dynamic digital circuits due to noise pulses.

The fundamental concepts of digital noise such as static and dynamic noise margins were reviewed. The noise tolerance metrics and existing noise tolerance techniques were also described.

It has been proposed and developed a new noise tolerant dynamic circuit technique. This new technique is easy to implement in dynamic precharge-evaluate gates like TSPC or Domino. The noise immunity increment with this new technique is much higher compared with the noise immunity of conventional dynamic gates and with dynamic gates implemented with previous noise tolerant dynamic circuit techniques.

The new noise tolerant technique uses two strategies to improve the noise tolerance of dynamic gates: first, rising the noise threshold of the gate by precharging an internal node in the PDN. Due to body effect the threshold voltage of the NMOS transistor, whose source has been precharged, is increased. Accordingly, the noise threshold of the gate is increased. Second, by isolating the dynamic node from the inputs when the PDN has been evaluated. This is achieved when the transparency window ends. These two strategies work to give additional noise immunity into a dynamic gate.

The advantages of this new noise tolerant dynamic circuit technique are listed as follows: (1) the high noise immunity reached when precharge-evaluate gates are implemented with this new technique, (2) the flexibility to implement the proposed technique in a wide variety of dynamic logic styles, (3) the pull down network of the gates is not modified to rise the noise immunity, (4) noise immunity and delay trade-off can be balanced to meet a specific delay, (5) this new technique preserves its noise immunity levels for large fan-in gates, and (6) these advantages are kept when technology scales.

Due to the two strategies used in the proposed noise tolerant technique the noise immunity levels (given by noise immunity curves, ANTE and UNG metrics), are much better than the levels of the conventional dynamic logic and some existing noise tolerant techniques. This fact makes this new technique an efficient solution for the signal integrity problem in deep-submicron circuits.

The proposed technique has the flexibility to be implemented in several dynamic logic styles like TSPC or Domino without any modification to the pull-down network of the gates. In general, the new noise tolerant technique is useful for precharge-evaluate circuits in heavily pipelined systems. Other advantage of the new technique is that the delay circuitry can be shared by two or more gates in the same pipeline stage. This results in both area and power consumption reduction.

The pull-down network of the logic gates is not part of the noise tolerance circuitry when this technique is implemented. This is advantageous because no capacitive load is added at the inputs of the logic gates and the drivers of this inputs remain unchanged. Consequently, design time is saved when a system is improved with this technique.

In digital dynamic circuits there is always a trade-off between noise immunity and per-

formance. In the new proposed technique this trade-off is given mainly by the transparency window width. This transparency window is easily tuned by the delay circuitry. The minimum transparency window width is determined by the discharge time of the precharge node in a gate implemented with the new technique. Wide-OR gates have a noise immunity larger than large fan-in AND gates in the proposed technique because OR gates need almost the same transparency window size.

The proposed technique was compared with the conventional dynamic logic as well as other noise tolerant technique for several transistor lengths in the deep-submicron regime. The results show that the proposed technique has the best noise immunity for all transistor lengths.

Some limitations of the new noise tolerant technique are the delay and power consumption penalties, but these limitations are common to all noise tolerant dynamic circuit techniques. However, the delay penalty and the power consumption penalty can be minimized tunning the transparency window and sharing the delay circuitry with other gates.

The proposed noise tolerant technique is validated experimentally in a relatively complex test circuit (1-bit carry look-ahead full adder). This test circuit was designed and fabricated in a 0.35 μm AMS technology using Cadence tools in a CAD design flow. For normal operation the full adder was tested up to 200 MHz. Several data input patterns were applied to the inputs of the full adder resulting in a correct operation (the sum was right). In order to obtain noise immunity curves from the test circuit the inputs were set constant and the victim node was assure to be 0. Noise immunity curves were obtained injecting noise pulses with variable amplitude and width into the victim node of the test circuit. The resulting noise immunity curves show an improvement in noise immunity of the proposed technique with respect to a conventional dynamic full adder. This fact verifies the effectiveness of the new noise tolerant technique. Also, this test circuit was useful to verify that the new noise tolerant dynamic circuit technique can be implemented in a pipelined circuit, increasing its noise immunity.

Finally, an improvement of the proposed technique is presented and its noise tolerance and performance are compared with conventional dynamic logic. Using the UNG metric it was found that a 2-input AND gate with this improved technique has a comparable noise immunity than the original proposed technique with less delay penalty. These results encourage further analysis on this improved technique. With the noise tolerant dynamic circuit techniques presented in

this work noise issues can be reduced in noisy systems with slight performance penalties in the deep-submicron era.

6.1 Future Work

Future work is directed towards the implementation of the proposed noise tolerant dynamic circuit technique into a relatively complex system like a data path. This implementation will allow to experimentally verify the proposed technique dependence on the fan-in and on the number of gates being affected by a noise pulse. A design methodology will be necessary to implement complex circuits with the proposed technique. This design methodology will improve noise tolerance of digital circuits minimizing performance penalties. The improved proposed technique needs to be analyzed in more detail. Extensive simulations and comparisons with other techniques are necessary to validate this new topology. Finally, more simple but accurate analytical expressions for noise immunity in digital dynamic circuits are needed.

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Resumen

La presente tesis trata sobre el problema del ruido de acoplamiento capacitivo en los circuitos dinámicos digitales. Se presenta una revisión de las lógicas dinámicas altamente susceptibles al ruido, donde se explican sus ventajas y desventajas desde el punto de vista de su desempeño. Se revisan los conceptos básicos del ruido mismo, márgenes de ruido y tolerancia e inmunidad al ruido en los circuitos digitales. Se explican las métricas existentes de tolerancia al ruido, cuyo uso es necesario para cuantificar la tolerancia al ruido de los circuitos dinámicos digitales. Se revisan las técnicas de tolerancia al ruido existentes y se describen sus mecanismos de tolerancia al ruido así como sus ventajas y desventajas.

Se analizan los efectos del ruido de acoplamiento capacitivo sobre el retardo, consumo de potencia e integridad de las señales de datos en las compuertas lógicas. Se propone una nueva técnica de tolerancia al ruido para circuitos dinámicos y se muestra su eficiencia para incrementar la tolerancia al ruido de los circuitos dinámicos digitales y en la mayoría de los casos supera a las ya existentes. Su estructura, así como su funcionamiento y mecanismos de tolerancia, se describen ampliamente. También se estudia el desempeño y optimización de esta nueva técnica para varios tipos de compuertas. Esta nueva propuesta se compara con algunas recientemente publicadas usando distintas compuertas dinámicas y tomando como parámetros de comparación el consumo de potencia, retardo y tolerancia al ruido, principalmente. Los resultados indican una mejora significativa en la tolerancia al ruido de la nueva técnica propuesta, lo que significa que se pueden soportar mayores niveles de ruido en las entradas de las compuertas dinámicas usando esta técnica. Para comprobar la eficiencia y flexibilidad de la técnica propuesta, se exponen varios ejemplos de aplicación para distintos tipos de compuertas y lógicas dinámicas.

También se analiza la tolerancia al ruido de varios registros dinámicos implementados

con la nueva propuesta y otra existente ante el escalamiento tecnológico. Los resultados de este análisis demuestran que aunque la tolerancia al ruido de los circuitos se está escalando junto con las tecnologías, la nueva técnica propuesta mantiene sus ventajas frente a las ya existentes. Este hecho es de gran relevancia ya que problemas de ruido serán cada vez mayores a medida que se escala la tecnología de circuitos integrados.

Se describe brevemente una topología modificada de la técnica y se hace un análisis de su desempeño. Los primeros resultados indican que la tolerancia al ruido de esta técnica modificada de tolerancia al ruido sigue siendo mejor que la de las previamente publicadas.

Finalmente, se presenta un circuito de pruebas fabricado con una tecnología CMOS de 0.35 μm. Con este circuito se valida la técnica propuesta en términos de desempeño y funcionalidad. Se verifica su correcta operación así como su tolerancia al ruido. Los resultados indican que se pueden alcanzar niveles de tolerancia al ruido mayores que los actuales usando la nueva técnica.